Programmes After Market Services
NSB-5 Series Transceivers

System Module

Issue 1 03/01

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System Connector

This section describes the electrical connection and interface levels between the base-band, RF and UI parts. The electrical interface specifications are collected into tables that cover a connector or a defined interface.

The system connector includes the following parts:

– DC connector for external plug–in charger and a desktop charger

– System connector for accessories and intelligent battery packs

The System connector is used to connect the transceiver to accessories.

System connector pins can be used to connect intelligent battery packs to the trans-ceiver.

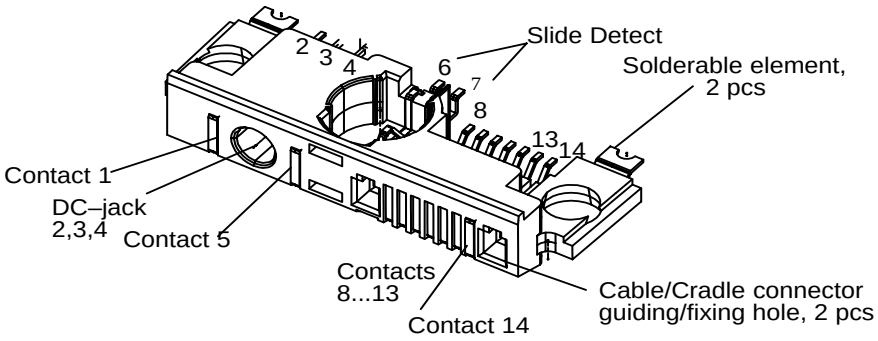


Figure 1: System connector module

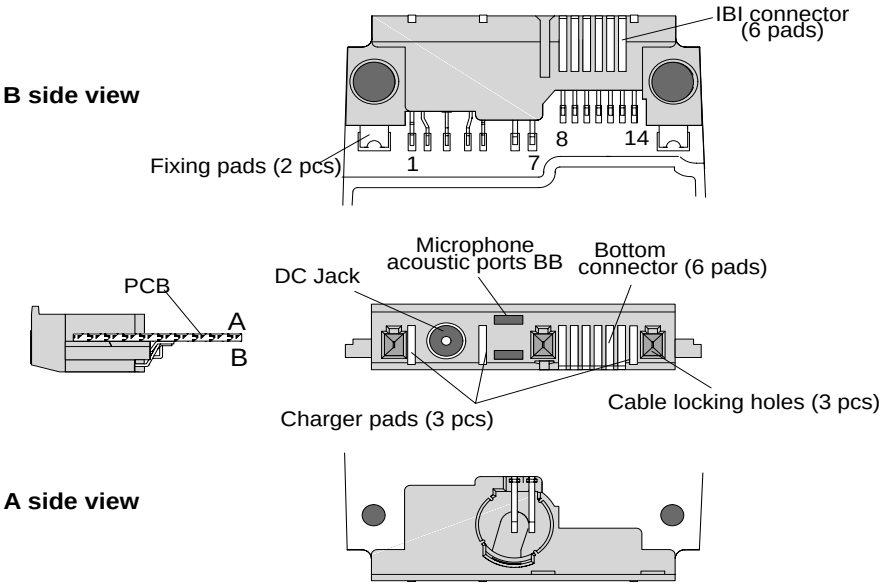


Figure 2: System Connector - detailed

Table 1: System connector signals

Pin	Name	Function	Description
1	V_IN	Bottom charger contacts	Charging voltage
2	L_GND	DC Jack	Logic and charging ground
3	V_IN	DC Jack	Charging voltage
4	CHRG_CTRL	DC Jack	Charger control
5	CHRG_CTRL	Bottom charger contacts	Charger control
6	MIC-P	Slide Detect Holder	Slide Detect
7	MIC-N	Slide Detect Holder	Gnd
8	XMIC	Bottom & IBI connectors	Analog audio input
9	SGND	Bottom & IBI connectors	Audio signal ground
10	XEAR	Bottom & IBI connectors	Analog audio output
11	MBUS	Bottom & IBI connectors	Bidirectional serial bus
12	FBUS_RX	Bottom & IBI connectors	Serial data in
13	FBUS_TX	Bottom & IBI connectors	Serial data out
14	L_GND	Bottom charger contacts	Logic and charging ground

DC Connector

The electrical specifications in Table 3 shows the idle voltage produced by the acceptable chargers at the DC connector input. The absolute maximum input voltage is 18V due to the transient suppressor that is protecting the charger input.

Slide Microphone

The microphone is connected to the slide by means of springs it has a microphone input level specified in Table 2. The microphone requires bias current to operate which is generated by the COBBA_GJP ASIC.

Slide Connector

An Interrupt signal to MAD2WD1 determines whether the slide is in an open or closed position.

Roller Interface

A mechanical solution is implemented and three interrupts are fed to the MAD2WD1.

Keys and Keymatrix

0–9, *, #, send, end, soft_1, soft_2, power_on_off, roller_push,

Headset Connector

The external headset device is connected to the system connector, from which the signals are routed to COBBA_GJP microphone inputs and earphone outputs.

Table 2: Mic signals of the system connector

NA	MICN mounted in slide	0	2	12.5	mV	Connected to COBBA_GJP MIC2N input. The maximum value corresponds to 1 kHz, 0 dBmO network level with input amplifier gain set to 32 dB, typical value is maximum value - 16 dB.
NA	MICP mounted in slide	0	2	12.5	mV	Connected to COBBA_GJP MIC2P input. The maximum value corresponds to 1 kHz, 0 dBmO network level with input amplifier gain set to 32 dB, typical value is maximum value - 16 dB.

Table 3: System/IBI connector

Pin	IB-pin	NAME	Function	Min	Typ	Max	Unit	Description
10	Yes	XEAR	Analog audio output (from phone to accessory)		47		Ω	Output AC impedance (ref GND) resistor tol. is 5%
					10		uF	Series output capacitance
				16		300	Ω	Load AC impedance to GND: Headset
				4.7	10		kΩ	Load AC impedance to SGND: External accessory
					1.0		V_{p-p}	Max. output level. No load
					100		kΩ	Resistance to accessory ground (in accessory)
			Accessory detection (from accessory to phone)		0.5		V	DC voltage (ref. SNGD). External accessory
					6.8		kΩ	Load DC resistance to SGND. External accessory
				0		0.2	V	DC voltage (ref SGND). Headset with closed switch
				16		1500	Ω	Load DC resistance to SNGD. Headset with closed switch
					2.8		V	DC voltage (ref SGND). No accessory or headset with open switch
					47		kΩ	Pull-up resistor to VBB in phone

Table 3: System/IBI connector

Pin	IB-pin	NAME	Function	Min	Typ	Max	Unit	Description
8	Yes	XMIC	Analog audio input (from accessory to phone)	2.0		2.2	kΩ	Input AC impedance
					100		Ω	Accessory source AC impedance
						1	V_{p-p}	Maximum signal level
			Headset micro-phone input (from accessory to phone)	2.0		2.2	kΩ	Input AC impedance
					2.5		kΩ	Headset source AC impedance
				100		600	µA	Bias current
						200	mV p-p	Maximum signal level
			Accessory mute. Voltage compared to SGND. (from phone to accessory)	2.5		2.9	V	Not muted
				0		1.55	V	Muted, without headset
				1.6	2.0	2.4	V	Comparator reference in accessory
			Headset detection (from accessory to phone) (NO TAG)	1.47		2.9	V	No headset (ref SGND)
				0		1.33	V	Headset connected (ref SGND)
					49		kΩ	Pull-up resistor to VBB in phone
			Function DLR-3 Datacable Detection	440		733	mV	DLR-3 detected (ref SGND)
9	Yes	SGND	Audio signal ground. Separated from phone GND (from phone to accessory)		47		Ω	Output AC impedance (ref GND)
					10		µF	Series output capacitance
					380		Ω	Resistance to phone ground (DC) (in phone)
					100		kΩ	Resistance to accessory ground (in accessory)
				-0.2		+0.2	V	DC voltage compared to phone GND
				-5		+5	V	DC voltage compared to accessory GND

Table 3: System/IBI connector

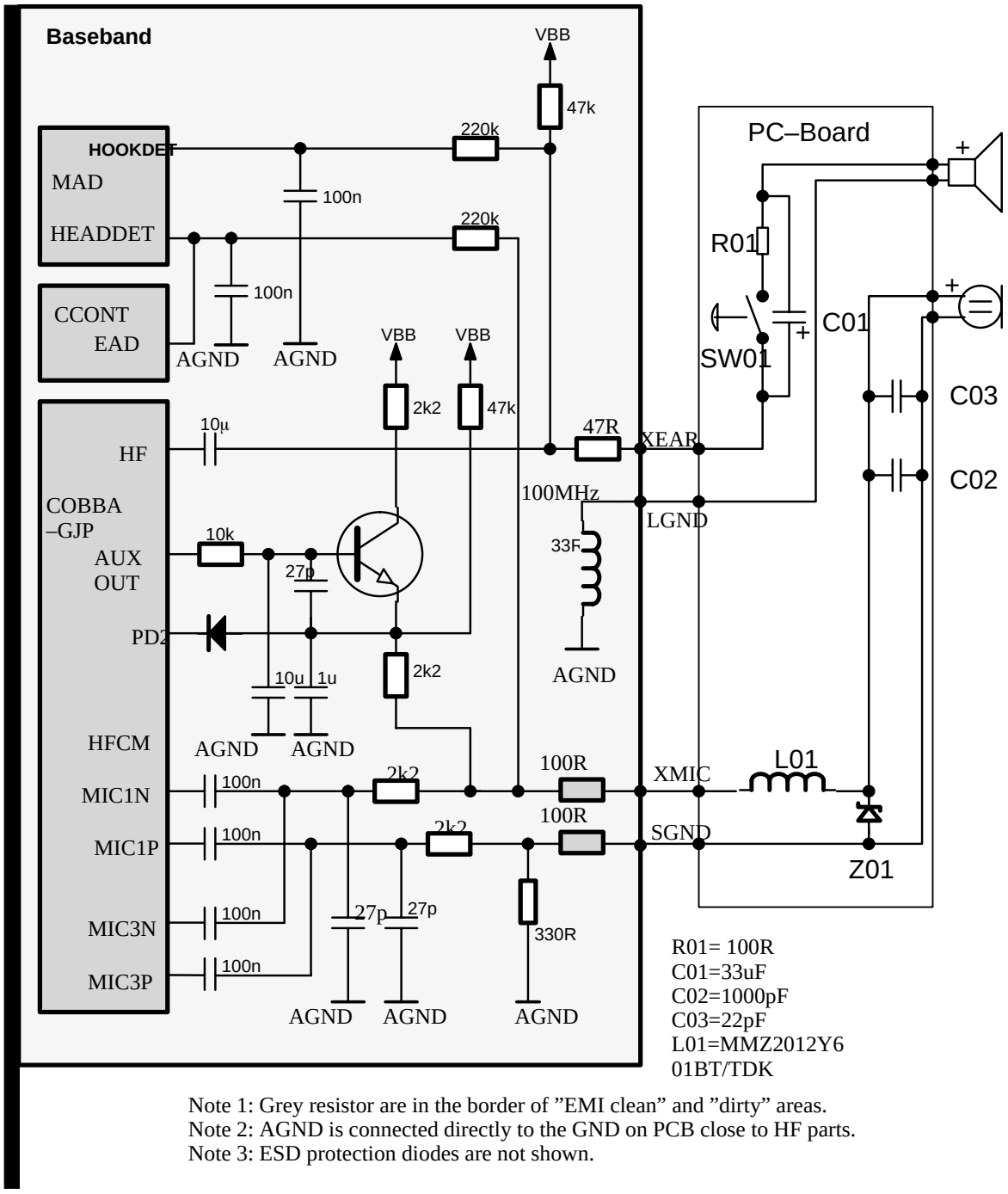
Pin	IB-pin	NAME	Function	Min	Typ	Max	Unit	Description
13	Yes	FBUS_TX	Serial data out (from phone to accessory)	0.1		0.8	V	Output low voltage @ I_{OL} ≤mA (ref GND)
				1.7		2.8	V	Output high voltage @ I_{OH} ≤4mA (ref GND)
					47		kΩ	Pull-up resistor in phone
					220		kΩ	Pull-down resistor in accessory
					47	100	Ω	Serial (EMI filtering) resistor in phone
						150	pF	Cable capacitance
						1	µs	Rise/fall time
12	Yes	FBUS_RX	Serial data in (from accessory to phone)	0		0.8	V	Input low voltage (ref GND)
				2.0		2.8	V	Input high voltage (ref GND)
					220		kΩ	Pull-down resistor in phone
					47		kΩ	Pull-up resistor in accessory
					2.2		kΩ	Serial (EMI filtering) resistor in accessory
						150	pF	Cable capacitance
						2	µs	Rise/fall time @ 115kbits/s
						1	µs	Rise/fall time @ 230kbits/s

Table 3: System/IBI connector

Pin	IB-pin	NAME	Function	Min	Typ	Max	Unit	Description
11	Yes	MBUS	Bidirec-tional serial bus	0		0.8	V	Input low voltage (ref GND)
				2.0		2.8	V	Input high voltage (ref GND)
		FLASH_ CLK		0		0.8	V	Output low voltage @ I_{OL} ≤4mA (ref GND)
				2.1		2.9	V	Output high voltage @ I_{OH} ≤100 µA (ref GND)
					4.7		kΩ	Pull-up resistor in phone
					220		kΩ	Pull-down resistor in accessory
					100		Ω	Serial (EMI filtering) resistor in phone
						200	pF	Cable capacitance
						5	µs	Rise/fall time @ 9600 bits/s
2, 14	-	L_GND	Logic and charging ground (separated from phone GND by EMI compo-nents)	0		1.0	A	Ground current
4,5	-	CHRG_ CTRL	Charger control (from phone to accessory)	0		0.8	V	Output low voltage @ I_{OL} ≤20 µA
				1.7		2.9	V	Output high voltage @ I_{OH} ≤20 µA
					32	37	Hz	PWM frequency
				1		99	%	PWM duty cycle
					20		kΩ	Serial (EMI filtering) resistor in phone
					30		kΩ	Pull-down resistor in phone

Table 3: System/IBI connector

Pin	IB-pin	NAME	Function	Min	Typ	Max	Unit	Description
1,3	-	VIN	Fast charger (from accessory to phone)	0		8.5	V	Charging voltage
				0		0.85	A	Charging current
						100	mV p-p	Ripple voltage @ f = 20...200Hz, load = 3 & 10 Ω
						100	mV p-p	Ripple voltage @ 4 = 0.2...30kHz, load = 3 & 10 Ω
						100	mV p-p	Ripple voltage @ f > 30kHz, load = 3 & 10 Ω
						200	mV p-p	Total ripple voltage @ f > 20Hz, load = 3 & 10 Ω
			Slow charger (from accessory to phone)	0		15	V_{peak}	Charging voltage (max. = unloaded, +20% overvoltage in mains)
				0		1.0	A_{peak}	Charging current (max. = shorted, +20% overvoltage in mains)



Note 1: Grey resistor are in the border of ”EMI clean” and ”dirty” areas.
Note 2: AGND is connected directly to the GND on PCB close to HF parts.
Note 3: ESD protection diodes are not shown.

Figure 3: Combined headset, system connector audio signals

Battery Connector

The BSI contact on the battery connector is used to detect when thebattery is removed with power switched on enabling the SIM card operation to shut down first. The BSI contact in the battery pack should be shorter than the supply power contacts to give enough time for the SIM shut down.

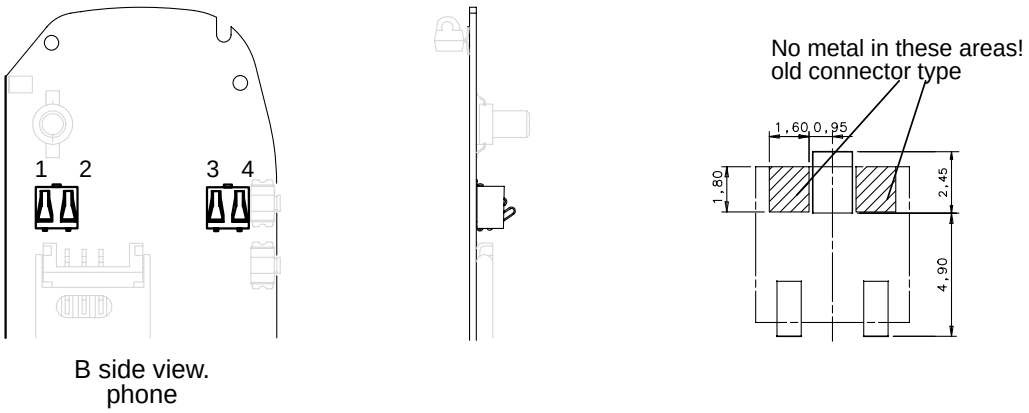


Figure 4: Battery connector locations

1	+VBATT
2	BSI
3	BTEMP
4	-VBATT

Vibra Alerting Device

A special battery pack contains a vibra motor. The vibra is controlled with one PWM signal by the MAD2WD1 via the BTEMP battery terminal.

SIM Card Connector

The SIM card connector is located on the PCB. Only small SIM cards are supported.

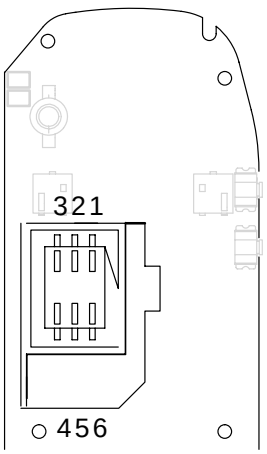


Figure 5: SIM Card Reader Ultra phone

Table 4: SIM Connector Electrical Specifications

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
1	GND	GND	0		0	V	Ground

Table 4: SIM Connector Electrical Specifications

Pin	Name	Parameter	Min	Typ	Max	Unit	Notes
2	VSIM	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Supply voltage
3	DATA	5V Vin/Vout 3V Vin/Vout	4.0 0 2.8 0	“1” “0” “1” “0”	VSIM 0.5 VSIM 0.5	V	SIM data Trise/Tfall max 1 us
4	SIMRST	5V SIM Card 3V SIM Card	4.0 2.8	“1” “1”	VSIM VSIM	V	SIM reset
5	SIMCLK	Frequency Trise/Tfall		3.25	 25	MHz ns	SIM clock
6	VPP	5V SIM Card 3V SIM Card	4.8 2.8	5.0 3.0	5.2 3.2	V	Programming voltage pin6 and pin2 tied together

VSIM supply voltages are specified to meet type approval requirements regardless of the tolerances in components.

Infrared Transceiver Module

An infrared transceiver module is designed as a substitute for hardwired connections between the phone and a PC. The infrared transceiver module is a stand alone component. In DCT3 the module is located inside and at the top of the phone.

The Rx and Tx is connected to the FBUS via a dual bus buffer. The module and buffer is activated from the MAD2 with a pull up on IRON. The Accif in MAD2 performs pulse encoding and shaping for transmitted data pulses and detection and decoding for received data pulses.

The data is transferred over the IR link using serial FBUS data at speeds 9.6, 19.2, 38.4, 57.6 or 115.2 kbits/s, which leads to maximum throughput of 92.160 kbits/s. The used IR module complies with the IrDA SIR specification (Infra Red Data Association), which is based on the HP SIR (Hewlett–Packard‘s Serial Infra Red) concept.

The following figure gives an example of IR transmission pulses. In IR transmission, a light pulse corresponds to 0–bit and a ”dark pulse” corresponds to 1–bit.

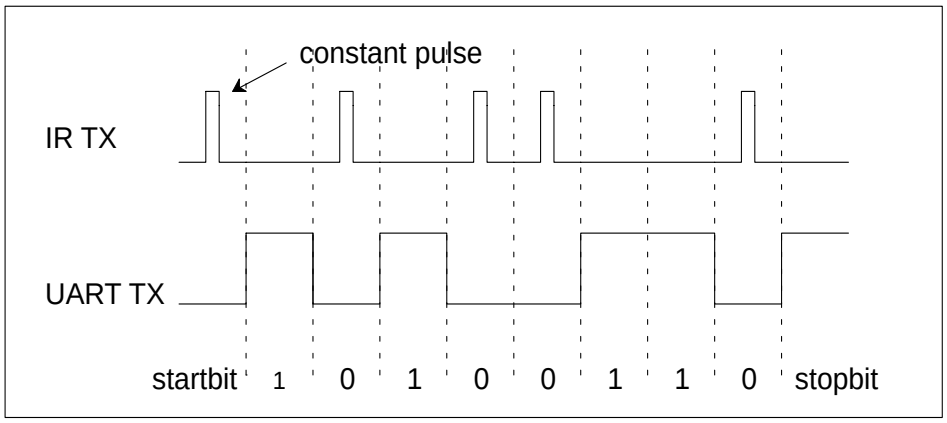


Figure 6: IR tramsmission frame - example

The FBUS cannot be used for external accessory communication, when the infrared mode is selected. Infrared communication reserves the FBUS completely.

Real Time Clock

Requirements for a real time clock implementation are a basic clock (hours and minutes), a calender and a timer with alarm and power on/off –function and miscellaneous calls. The RTC will contain only the time base and the alarm timer but all other functions (e.g. calendar) will be implemented with the MCU software. The RTC needs a power backup to keep the clock running when the phone battery is disconnected. The backup power is supplied from a rechargable polyacene battery that can keep the clock running for approximately ten minutes. If the backup has expired, the RTC clock restarts after the main battery is connected. The CCONT resets the MCU in approx 62ms and the 32kHz source is settled (after approx. 1s).

The CCONT is an ideal place for an integrated real time clock as the asic already contains the power up/down functions and a sleep control with the 32kHz sleep clock, which is always running when the phone battery is connected. This sleep clock is used for a time source to a RTC block.

Baseband Module

Technical Summary

The baseband architecture is basically similar to DCT3 GSM phones. DCT3.5 differs from DCT3 in the single PCB concept and the serial interface between MAD2WD1 and COBBA_GJP and MAD2WD1 and CCONT. In DCT3.5 the MCU, the system-specific ASIC and the DSP are intergrated into one ASIC, called the MAD2WD1 chip, which takes care of all the signal processing and operation controlling tasks of the phone.

The baseband architecture supports a power saving function called ”sleep mode”. This sleep mode shuts off the VCTCXO, which is used as system clock source for both RF and baseband. During the sleep mode the system runs from a 32 kHz crystal. The phone is wakened up by a timer running from this 32 kHz clock supply. The sleeping time is deter-

mined by some network parameters. When the sleep mode is entered both the MCU and the DSP are in standby mode and the normal VCTCXO clock has been switched off.

The battery voltage range in DCT3 family is 3.0V to 4.5V depending on the battery charge and used cell type (Li–Ion or NiMH). Because of the lower battery voltage the baseband supply voltage is lowered to a nominal of 2.8V.

The baseband is running from a 2.8V power rail which is supplied by a power controlling asic (CCONT). In the CCONT there are seven individually controlled regulator outputs for the RF section, one 2.8V output for the baseband plus a core voltage for MAD2WD1. However this is not used in NSB–5 because the chipset supports 2.8 Volts. In addition there is one +5V power supply output(V5V). TheCCONTalso contains a SIM interface which supports both 3V and 5V SIM cards. A real time clock function is integrated into the CCONT which utilizes the same 32KHz clock supply as the sleep clock. A backup power supply is provided for the RTC, which keeps the real time clock running when the main battery is removed. The backup power supply is a rechargeable polyacene battery with a backup time of ten minutes.

The interface between the baseband and the RF section is handled by a specific asic. The COBBA_GJP asic provides A/D and D/A conversion of the in–phase and quadrature receive and transmit signal paths and also A/D and D/A conversions of received and transmitted audio signals to and from the UI parts. Data transmission between the COBBA_GJP and the MAD2WD1 is implemented using serial connections. Digital speech processing is handled by the MAD2WD1 asic. The COBBA_GJP asic is a dual supply voltage circuit, the digital parts are running from the baseband supply VBB and the analog parts are running from the analog supply VCOBBA (VR6).

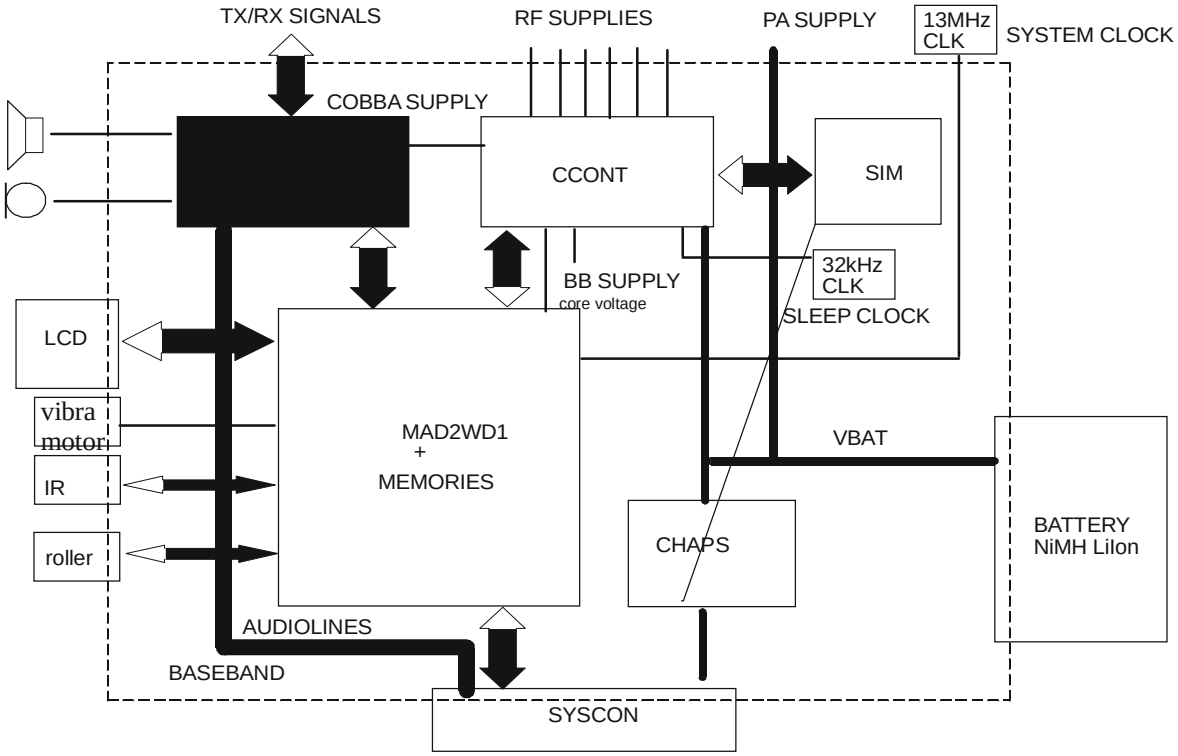


Figure 7: Block Diagram

Power Distribution

In normal operation the baseband is powered from the phone's battery. The battery consists of one Lithium–Ion cell. There is also a possibility to use batteries consisting of three Nickel Metal Hydride cells or one solid state cell. An external charger can be used for recharging the battery and supplying power to the phone. The charger can be either so called fast charger, which can deliver supply current up to 1600 mA or a standard charger that can deliver approx 300 mA.

The CCONT provides voltage to the circuitry excluding the RF PA, LCD, and IrDa, which are supplied via a continuous power rail direct from the battery. The RF PA module has a cutoff voltage of 3.1V. The battery*(see note)* feeds power directly to several parts of the system: CCONT, PA, and UI circuitry (display lights, buzzer). The four dedicated control lines, RxPwr, TxPwr, SIMCardPwr, and SynthPwr from MAD2 to CCONT have changed to a serial control signal between MAD2WD1 and CCONT. Figure 8 shows a simplified block diagram of the power distribution.

Note : In battery terms there is VBATT and VB, the difference is a filter (coil and capacitors).

The power management circuitry provides protection against overvoltages, charger failures, and pirate chargers, etc., that could cause damage to the phone.

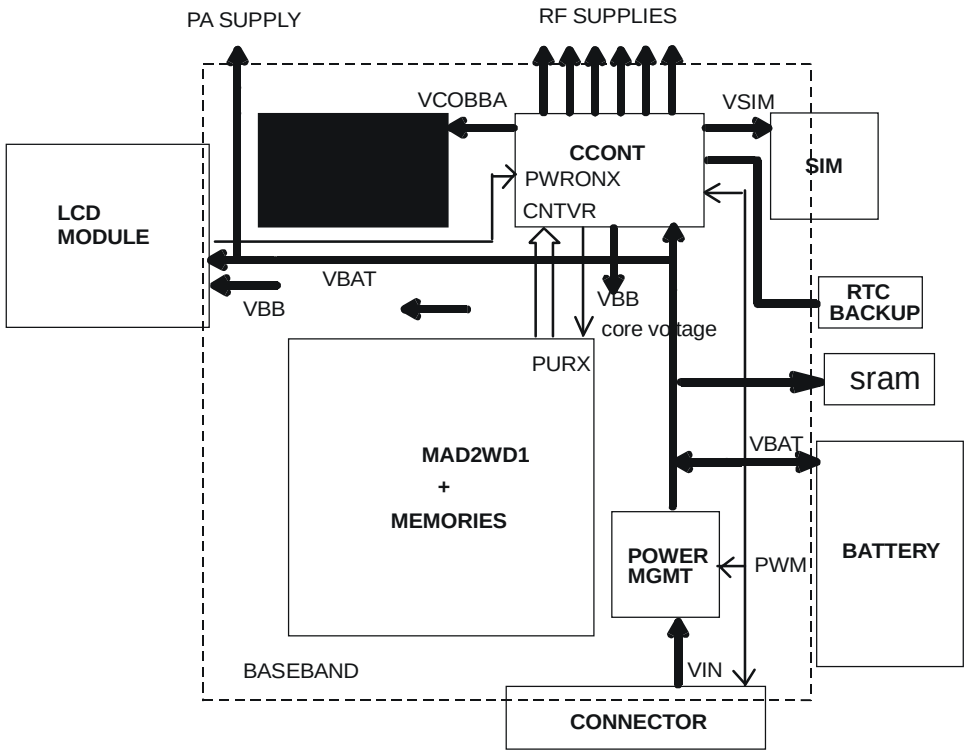


Figure 8: Baseband power distribution

The heart of the power distribution is the CCONT. It includes all the voltage regulators and feeds the power to most of the system. The whole baseband is powered from the same regulator which provides 2.8V baseband supply VBB. The baseband regulator is active always when the phone is powered on. The core baseband regulator feeds, amongst others, MAD2WD1 and memories, COBBA_GJP digital parts and the LCD driver in the UI section. COBBA_GJP analog parts are powered from a dedicated 2.8V supply

VCOBBA by the CCONT. There is a separate regulator for a SIM card which is selectable between 3V and 5V and controlled by the SIMPwr line from MAD2WD1 to CCONT.

The CCONT contains a real time clock function, which is powered from a RTC backup when the main battery is disconnected. The RTC backup is rechargable polyacene battery.

CCONT includes also six additional 2.8V regulators providing power to the RF section. These regulators can be controlled by the seriel interface from MAD2WD1; i.e., RF regulator control register in CCONT which MAD2WD1 can update.

CCONT supplies a core voltage to the MAD2WD1. The core voltage is by default 1.975V, but can be set lower, depending on the MAD2 silicon technology.

RAM_BCK is not used.

CCONT generates also a 1.5 V reference voltage VREF to COBBA_GJP, SUMMA. The VREF voltage is also used as a reference to some of the CCONT A/D converters and as a reference for al the other regulators.

In addition to the above-mentioned signals, MAD2WD1 includes also TXP control signal which goes to SUMMA power control block and to the power amplifier. The transmitter power control TXC is led from COBBA_GJP to SUMMA.

Table 5: CCONT current output capability/nominal voltage

Regulator	Maximum current	Unit	Vout	Unit	Notes
VR1	25	mA	2.8	V	VCTCXO
VR2	25	mA	2.8	V	CRFU Rx
VR3/switch	50	mA	2.8	V	PLL VSYN
VR4	90	mA	2.8	V	VCO VSYN
VR5	80	mA	2.8	V	SUMMA Rx
VR6	100	mA	2.8	V	COBBA_GJP
VR7	150	mA	2.8	V	SUMMA+CRFU Tx
VBB ON VBB SLEEP	125 1	mA mA	2.8 2.8	V V	current limit 250mA current limit 5mA
VSIM	30	mA	3.0/ 5.0	V V	VSIM outout voltage selectable
V_core	50	mA	1.975	V	programmable core supply for CPU/ DSP/SYS ASIC dV=225V
V_RAM_bck/VR3	50	mA	2.8	V	normal mode 2.8V. 2.0V for data retention. (not used)

VSIM must fulfill the GSM11.10 current spike requirements.

VSIM and V5V can give a total of 30 mA.

Power Up

The baseband is powered up by:

1 Pressing the power key, that generates a PWRONX interrupt signal from the power key to the CCONT, which starts the power up procedure.

2 Connecting a charger to the phone. The CCONT recognizes the charger from the VCHAR voltage and starts the power up procedure.

3 A RTC interrupt. If the real time clock is set to alarm and the phone is switched off, the RTC generates an interrupt signal, when the alarm is gone off. The RTC interrupt signal is con-nected to the PWRONX line to give a power on signal to the CCONT just like the power key.

4 A battery interrupt. Intelligent battery packs have a possibility to power up the phone. When the battery gives a short (10ms) voltage pulse through the BTEMP pin, the CCONT wakes up and starts the power on procedure.

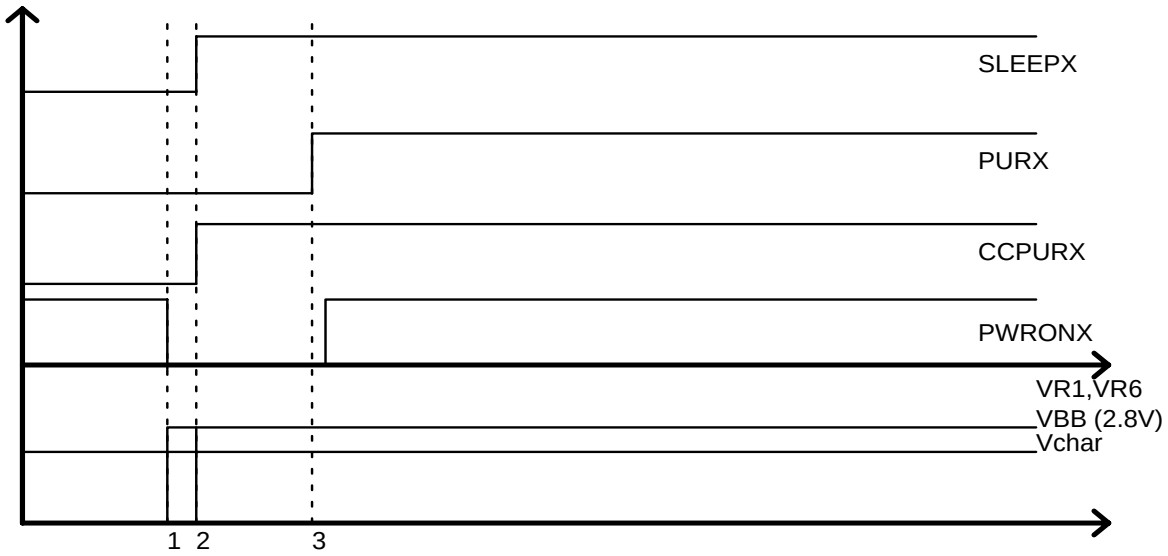
Power up with a charger

When the charger is connected, CCONT will switch on the CCONT digital voltage as soon as the battery voltage exeeds 3.0V. The reset for CCONT's digital parts is released when the operating voltage is stabilized (50 us from switching on the voltages). Operating voltage for VCXO is also switched on. The counter in CCONT digital section will keep MAD in reset for 62 ms (PURX) to make sure that the clock provided by VCXO is stable. After this delay, MAD reset is released, and VCXO–control (SLEEPX) is given to MAD. The diagram assumes empty battery, but the situation would be the same with full battery:

When the phone is powered up with an empty battery pack using the standard charger, the charger may not supply enough current for standard power-up procedure and the powerup must be delayed.

Power Up With the Power Switch (PWRONX)

When the power on switch is pressed the PWRONX signal will go low. CCONT will switch on the CCONT digital section and VCXO as was the case with the charger-driven power up. If PWRONX is low when the 64 ms delay expires, PURX is released and SLEEPX control goes to MAD. If PWRONX is not low when 64 ms expires, PURX will not be released, and CCONT will go to power off (digital section will send power off signal to analog parts).



1: Power switch pressed ==> Digital voltages on in CCONT (VBB).

2: CCONT digital reset released. VCXO turned on.

3: 62 ms delay to see if power switch is still pressed.

Power Up by RTC

RTC (internal in CCONT) can power the phone up by changing RTCPwr to logical ”1”. RTCPwr is an internal signal from the CCONT digital section.

Power Up by IBI

IBI can power CCONT up by sending a short pulse to logical ”1”. RTCPwr is an internal signal from the CCONT digital section.

Acting Dead

If the phone is off when the charger is connected, the phone is powered on but enters a state called ”acting dead”. To the user the phone acts as if it was switched off. A battery charging alert is given and/or a battery charging indication on the display is shown to acknowledge the user that the battery is being charged.

Active Mode

In the active mode the phone is in normal operation, scanning for channels, listening to a base station, transmitting and processing information. All the CCONT regulators are operating. There are several substates in the active mode depending on if the phone is in burst reception, burst transmission, if DSP is working etc.

Sleep Mode

In the sleep mode all the regulators except the baseband VBB, Vcore, and the SIM card VSIM regulators are off. Sleep mode is activated by the MAD2WD1 after MCU and DSP clocks have been switched off. The voltage regulators for the RF section are switched off

and the VCXO power control, VCXOPwr is set low. In this state only the 32 kHz sleep clock oscillator in CCONT is running. The flash memory power down input is connected to the VCXO power control, so that the flash is deep powered down during sleep mode. During sleep mode, the phone wakes up periodically to page the base station for incoming calls, location update, etc. The paging rate is a parameter set by the BS.

The sleep mode is exited either by the expiration of a sleep clock counter in the MAD2WD1 or by some external interrupt, generated by a charger connection, key press, headset connection, etc. The MAD2WD1 starts the wake up sequence and sets the VCXOPwr control high. After VCXO settling time other regulators and clocks are enabled for active mode.

If the battery pack is disconnect during the sleep mode, the CCONT shall power down the SIM in the sleep mode as there is no time to wake up the MCU.

Battery charging

The electrical specifications give the idle voltages produced by the acceptable chargers at the DC connector input. The absolute maximum input voltage is 30V due to the transient suppressor that is protecting the charger input. At phone end there is no difference between a plug–in charger or a desktop charger. The DC–jack pins and bottom connector charging pads are connected together inside the phone.

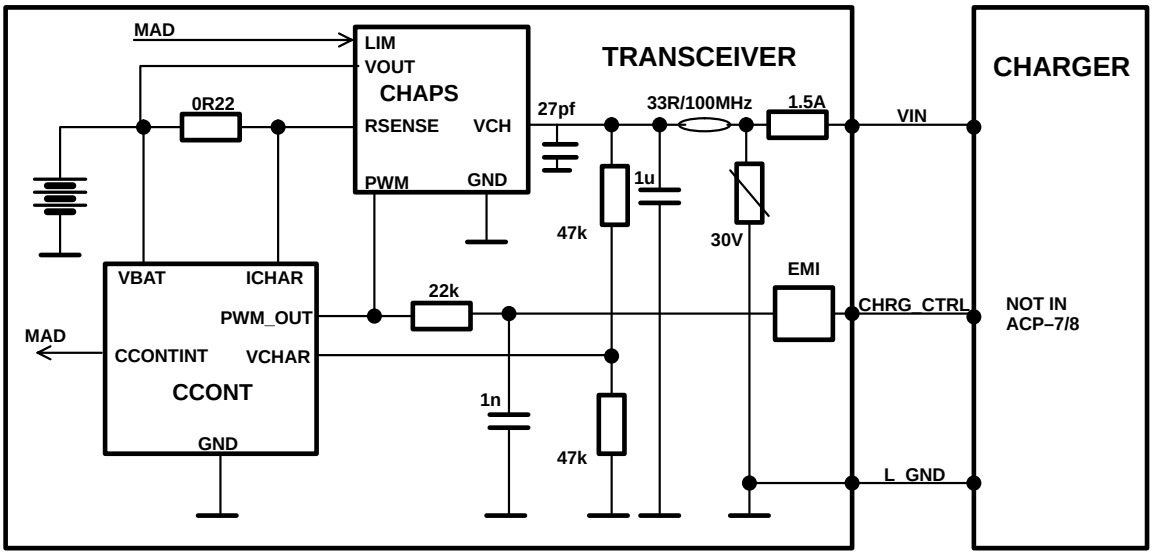


Figure 9: Battery Charging

Startup Charging

When a charger is connected, the CHAPS is supplying a startup current minimum of 130mA to the phone. The startup current provides initial charging to a phone with an empty battery. Startup circuit charges the battery until the battery voltage level reaches 3.0V (+/– 0.1V) and the CCONT releases the PURX reset signal and program execution starts. Charging mode is changed from startup charging to PWM charging that is controlled by the MCU software. If the battery voltage reaches 3.55V (3.75V maximum) before the program has taken control over the charging, the startup current is switched off. The startup current is switched on again when the battery voltage is sunken 100mV (nominal).

Table 6: Startup Charging Parameters

Parameter	Symbol	Min	Typ	Max	Unit
VOUT start-up mode cutoff limit	Vstart	3.45	3.55	3.75	V
VOUT start-up mode hysteresis Note: COUT = 4.7µF	Vstarthys	80	100	200	mV
Start-up regulator output current VOUT = 0V ... Vstart	Istart	130	165	200	mA

Battery Overvoltage Protection

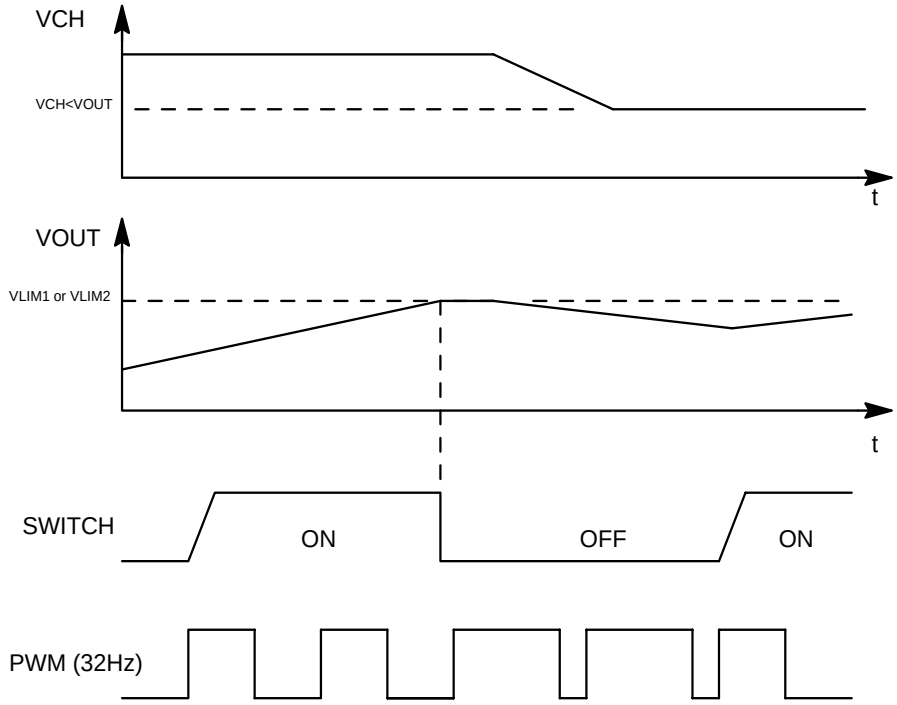
Output overvoltage protection is used to protect phone from damage. This function is also used to define the protection cutoff voltage for different battery types (Li or Ni). The power switch is immediately turned OFF if the voltage in VOUT rises above the selected limit VLIM1 or VLIM2.

Table 7: Battery Overvoltage Protection

Parameter	Symbol	LIM input	Min	Typ	Max	Unit
Output voltage cutoff limit (during transmission or Li-battery)	VLIM1	LOW	4.4	4.6	4.8	V
Output voltage cutoff limit (no transmission or Ni-battery)F	VLIM2	HIGH	4.8	5.0	5.2	V

The voltage limit (VLIM1 or VLIM2) is selected by logic LOW or logic HIGH on the CHAPS (N101) LIM– input pin. Default value is lower limit VLIM1.

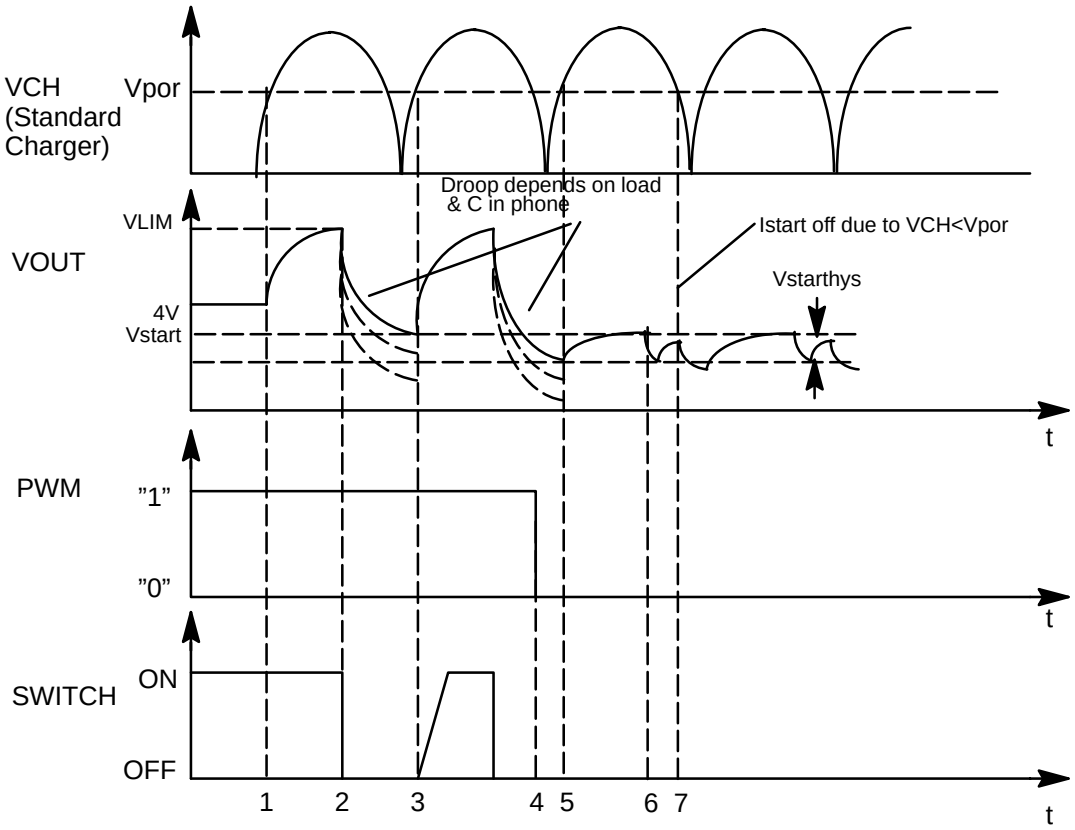
When the switch in output overvoltage situation has once turned OFF, it stays OFF until the the battery voltage falls below VLIM1 (or VLIM2) and PWM = LOW is detected. The switch can be turned on again by setting PWM = HIGH.



Battery Removal During Charging

Output overvoltage protection is also needed in case the main battery is removed when charger connected or charger is connected before the battery is connected to the phone.

With a charger connected, if VOUT exceeds VLIM1 (or VLIM2), CHAPS turns switch OFF until the charger input has sunken below Vpor (nominal 3.0V, maximum 3.4V). MCU software will stop the charging (turn off PWM) when it detects that battery has been removed. The CHAPS remains in protection state as long as PWM stays HIGH after the output overvoltage situation has occurred.



1 Battery removed, (standard) charger connected, VOUT rises (follows charger voltage)

2 VOUT exceeds limit VLIM(X), switch is turned immediately OFF

3 VOUT falls (because no battery), also VCH<Vpor (standard chargers full–rectified output). When VCH > Vpor and VOUT < VLIM(X) –> switch turned on again (also PWM is still HIGH) and VOUT again exceeds VLIM(X).

4 Software sets PWM = LOW –> CHAPS does not enter PWM mode

5 PWM low –> Startup mode, startup current flows until Vstart limit reached

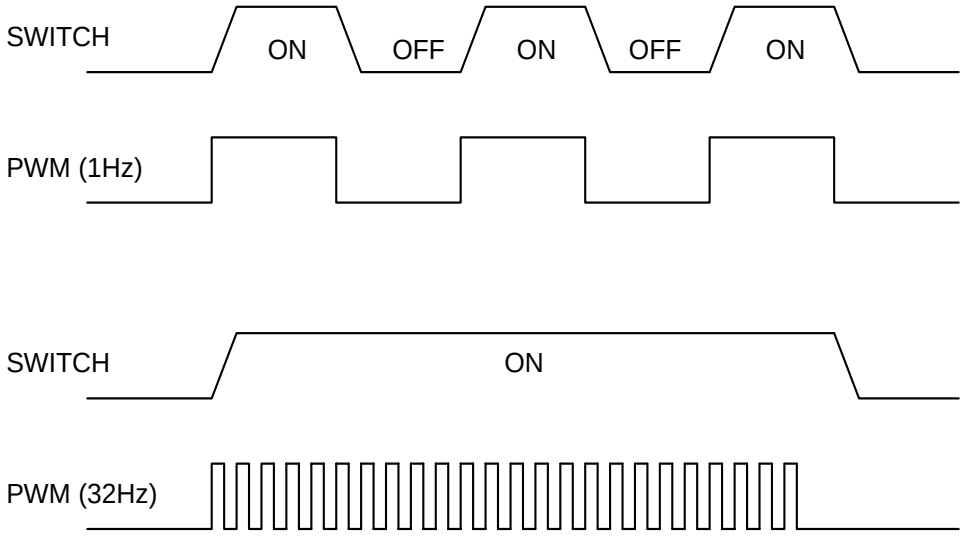
6 VOUT exceeds limit Vstart, Istart is turned off

7 VCH falls below Vpor

Different PWM Frequencies (1Hz and 32 Hz)

When a travel charger (2–wire charger) is used, the power switch is turned ON and OFF by the PWM input when the PWM rate is 1Hz. When PWM is HIGH, the switch is ON and the output current Iout = charger current – CHAPS supply current. When PWM is LOW, the switch is OFF and the output current Iout = 0. To prevent the switching transients inducing noise in audio circuitry of the phone soft switching is used.

The performance travel charger (3– wire charger) is controlled with PWM at a frequency of 32Hz. When the PWM rate is 32Hz CHAPS keeps the power switch continuously in the ON state.



Battery Identification

Different battery types are identified by a pulldown resistor inside the battery pack. The BSI line inside transceiver has a 100k pullup to VBB.

The MCU can identify the battery by reading the BSI line DC–voltage level with a CCONT (N100) A/D–converter.

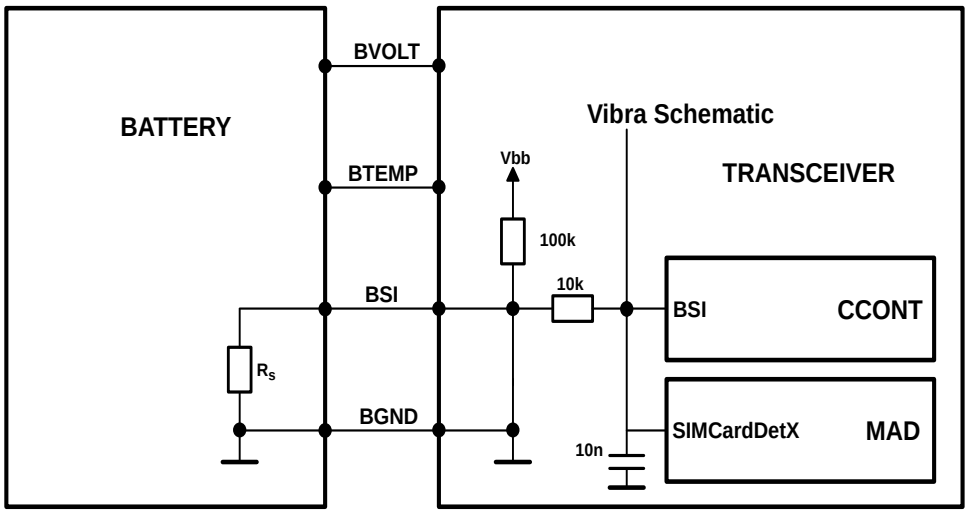
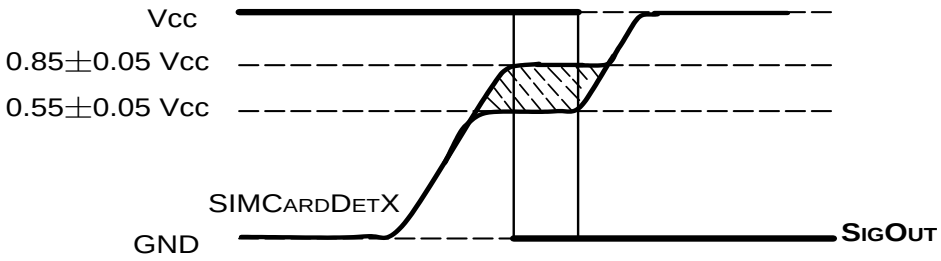


Figure 10: Battery Identification

The battery identification line is used also for battery removal detection. The BSI line is connected to a SIMCardDetX line of MAD2 (D300). SIMCardDetX is a threshold detector with a nominal input switching level 0.85xVcc for a rising edge and 0.55xVcc for a falling edge. The battery removal detection is used as a trigger to power down the SIM card before the power is lost. The BSI contact in the battery pack is made 0.7mm shorter than the supply voltage contacts so that there is a delay between battery removal detection

and supply power off.



Battery Temperature

The battery temperature is measured with a NTC inside the battery pack. The BTEMP line inside transceiver has a 100k pullup to VREF. The MCU can calculate the battery temperature by reading the BTEMP line DC–voltage level with a CCONT (N100) A/D–converter.

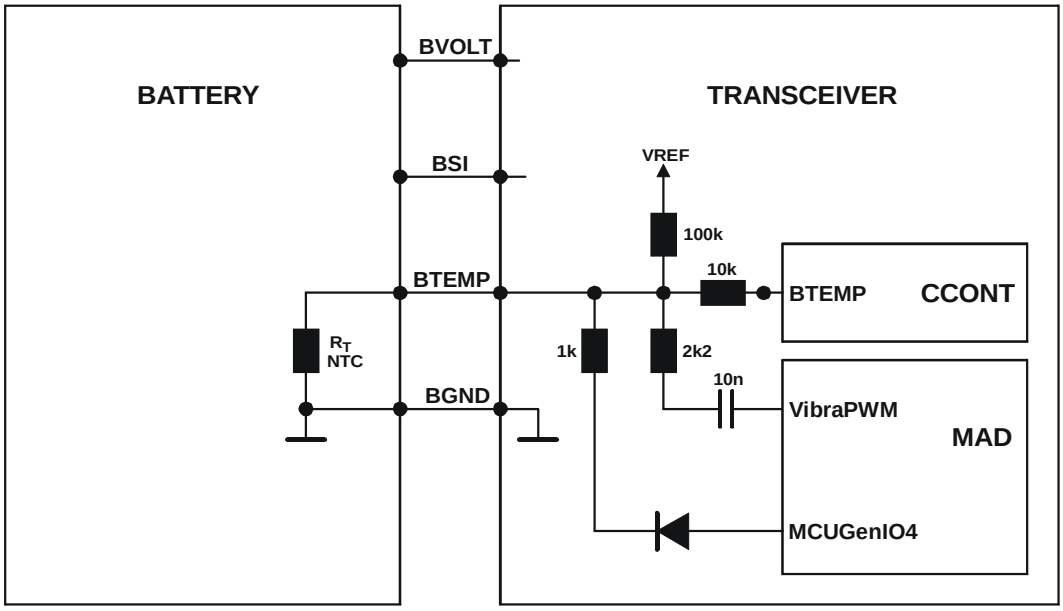


Figure 11: Battery Temperature

Supply Voltage Regulators

The heart of the power distrubution is the CCONT. It includes all the voltage regulators and feeds the power to the whole system. The baseband digital parts are powered from the VBB regulator which provides 2.8V baseband supply. The baseband regulator is active always when the phone is powered on. The VBB baseband regulator feeds MAD and memories, COBBA digital parts and the LCD driver in the UI section. There is a separate regulator for a SIM card. The regulator is selectable between 3V and 5V and controlled by the SIMPwr line from MAD to CCONT. The COBBA analog parts are powered from a dedicated 2.8V supply VCOBBA. The CCONT also supplies 5V for RF. The CCONT contains a real time clock function, which is powered from a RTC backup when the main battery is disconnected.

The RTC backup is rechargable polyacene battery, which has a capacity of 50uAh (@3V/2V) The battery is charged from the main battery voltage by the CHAPS when the main battery voltage is over 3.2V. The charging current is 200uA (nominal).

Table 8: Regulator States for Different Modes of Operation

Operating mode	Vref	RF REG	VCOBBA	VBB	VSIM	SIMIF
Power off	**Off**	Off	Off	Off	Off	Pull down
Power on	**On**	On/Off	On	On	On	On/off
Reset	**On**	Off VR1 On	On	On	On	Pull down
Sleep	**Off**	Off	Off	On	On	On/off

Note: CCONT includes five additional 2.8V regulators providing power to the RF section. These regulators can be controlled either by the direct control signals from MAD or by the RF regulator control register in CCONT which MAD can update. Below are the listed the MAD control lines and the regulators they control:

- TxPwr controls VTX regulator (VR7)
- RxPwr controls VRX regulators (VR2 and VR5)
- SynthPwr controls VSYN_1 and VSYN_2 regulators (VR1_SW and VR4)
VCXOPwr controls VXO regulator (VR1)

CCONT generates also a 1.5 V reference voltage VREF to COBBA, SUMMA, and CRFU. The VREF voltage is also used as a reference to some of the CCONT A/D converters.

In addition to the above-mentioned signals, MAD includes TXP control signal, which goes to SUMMA power control block and to the power amplifier. The transmitter power control TXC is led from COBBA to SUMMA.

Audio Control

The audio control and processing is handled by the COBBA–GJP, which contains the audio and RF codecs, and the MAD2, which contains the MCU, ASIC, and DSP blocks handling and processing the audio signals.

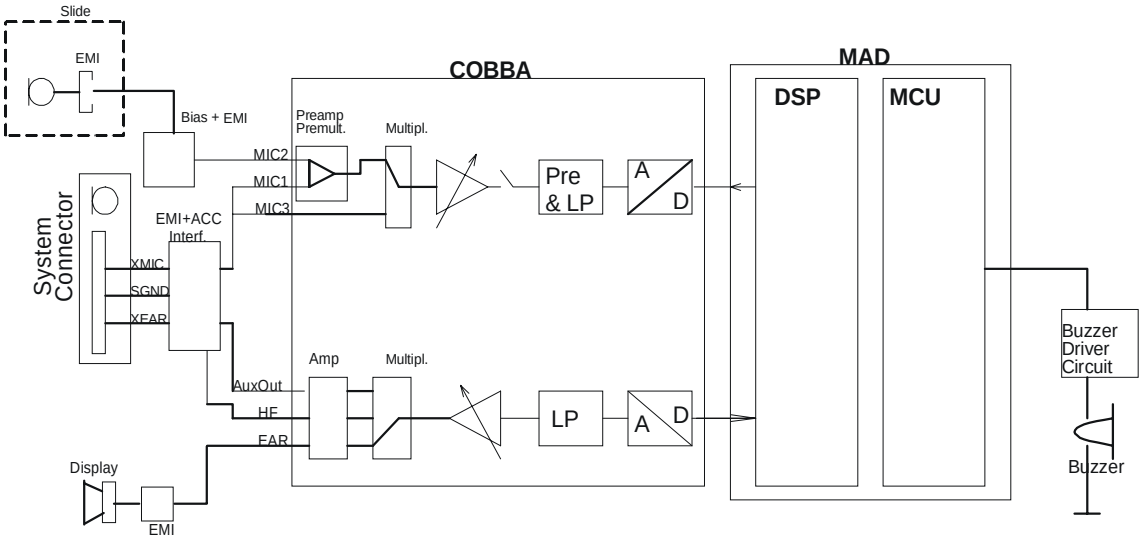


Figure 12: Audio Control

The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs at the COBBA–GJP asic. Inputs for the microphone signals are differential type.

The MIC1 inputs are used for a headset microphone that can be connected directly to the system connector. The internal microphone is connected to MIC2 inputs and an external pre–amplified microphone (handset/handfree) signal is connected to the MIC3 inputs. In COBBA there are also three audio signal outputs of which dual ended EAR lines are used for internal earpiece and HF line for accessory audio output. The third audio output AUX-OUT is used only for bias supply to the headset microphone. As a difference to DCT2 generation the SGND does not supply audio signal (only common mode). Therefore there are no electrical loopback echo from downlink to uplink.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. The output for the external accessory and the headset is single ended with a dedicated signal ground SGND. Input and output signal source selection and gain control is performed inside the COBBA–GJP asic according to control messages from the MAD2. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD2 and transmitted to the COBBA–GJP for decoding.

Internal Microphone and Earpiece

The baseband supports three microphone inputs and two earphone outputs. The inputs can be taken from an internal microphone, a headset microphone, or from an external microphone signal source. The microphone signals from different sources are connected to separate inputs to the COBBA_GJP asic. Inputs for the microphone signals are of a differential type.

External Audio Connections

The external audio connections are presented in figure 16. A headset can be connected directly to the system connector. The headset microphone bias is supplied from COBBA AUXOUT output and fed to microphone through XMIC line. The 330ohm resistor from SGND line to AGNDprovides a return path for the bias current.

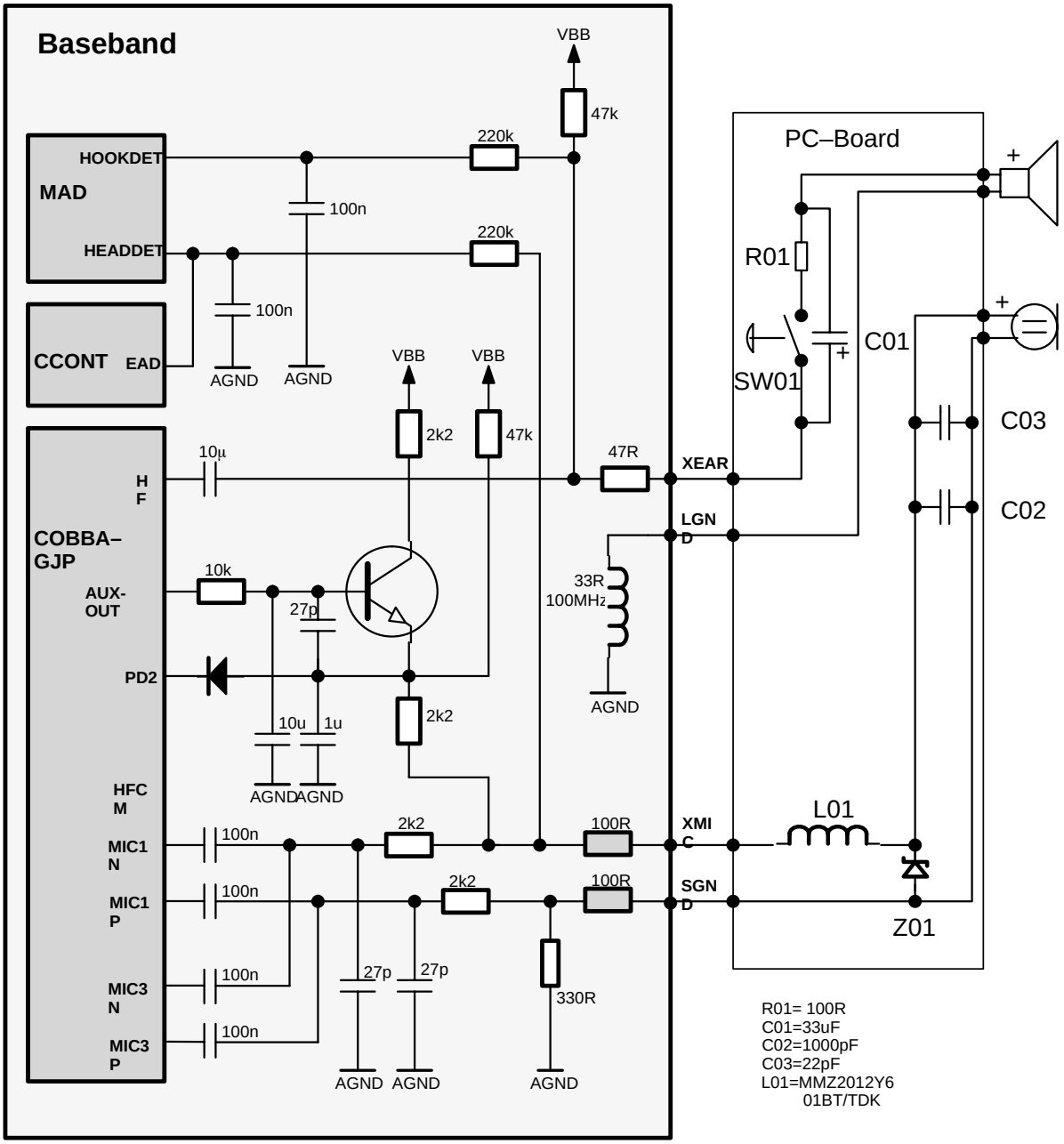


Figure 13: Combined headset and system connector audio signal

Analog Audio Accessory Detection

In XEAR signal there is a 47 kΩ pullup in the transceiver and 6.8 kΩ pull–down to SGND in accessory. The XEAR is pulled down when an accessory is connected, and pulled up when disconnected. The XEAR is connected to the HookDet line (in MAD), an interrupt is given due to both connection and disconnection. There is filtering between XEAR and HookDet to prevent audio signal giving unwanted interrupts.

External accessory notices powered–up phone by detecting voltage in XMIC line. In Table 9 there is a truth table for detection signals.

Table 9: HookDet/HeadDet Detection Truth Table

Accessory connected	HookDet	HeadDet	Notes
No accessory connected	High	HIgh	Pull-ups in the transceiver
Headset HDC-9 with a button switch pressed	Low	Low	XEAR and XMIC loaded (dc)
Headset HDC-9 with a button switch released	High	Low *)	XEAR unloaded (dc)
Handsfree (HFU-1)	Low	High	XEAR loaded (dc)

Internal Audio Connections

The speech coding functions are performed by the DSP in the MAD2 and the coded speech blocks are transferred to the COBBA–GJP for digital to analog conversion, down link direction. In the up link direction the PCM coded speech blocks are read from the COBBA–GJP by the DSP.

There are two separate interfaces between MAD2 and COBBA–GJP: a parallel bus and a serial bus. The parallel bus has 12 data bits, 4 address bits, read and write strobes, and a data available strobe. The parallel interface is used to transfer all the COBBA–GJP control information (both the RFI part and the audio part) and the transmit and receive samples. The serial interface between MAD2 and COBBA–GJP includes transmit and receive data, clock and frame synchronization signals. It is used to transfer the PCM samples. The frame synchronization frequency is 8 kHz which indicates the rate of the PCM samples and the clock frequency is 1 MHz. COBBA is generating both clocks.

4–wire PCM Serial Interface

The interface consists of following signals: a PCM codec master clock (PCMDClk), a frame synchronization signal to DSP (PCMSClk), a codec transmit data line (PCMTX), and a codec receive data line (PCMRX). The COBBA–GJP generates the PCMDClk clock, which is supplied to DSP SIO. The COBBA–GJP also generates the PCMSClk signal to DSP by dividing the PCMDClk. The PCMDClk frequency is 1.000 MHz and is generated by dividing the RFIClk 13 MHz by 13. The COBBA–GJP further divides the PCMDClk by 125 to get a PCMSClk signal, 8.0 kHz.

The output for the internal earphone is a dual ended type output capable of driving a dynamic type speaker. The output for the external accessory and the headset is single ended with a dedicated signal ground SGND. Input and output signal source selection and gain control is performed inside the COBBA_GJP asic according to control messages from the MAD2WD1. Keypad tones, DTMF, and other audio tones are generated and encoded by the MAD2WD1 and transmitted to the COBBA_GJP for decoding. MAD2WD1 generates two separate PWM outputs, one for a buzzer and one for vibra (internal and external via BTEMP).

Speech Processing

The speech coding functions are performed by the DSP in the MAD2WD1 and the coded speech blocks are transferred to the COBBA_GJP for digital to analog conversion, down link direction. In the up link direction the PCM coded speech blocks are read from the COBBA_GJP by the DSP.

There are two options for the PCM interface between MAD2WD1 and COBBA_GJP. The 4-pin solution and a 1-pin solution. The four pin serial interface between MAD2WD1 and COBBA_GJP includes transmit and receive data, clock and frame synchronization signals. It is used to transfer the PCM samples. The frame synchronization frequency is 8 kHz, which indicates the rate of the PCM samples and the clock frequency is 1 MHz. COBBA_GJP generates both clocks. NSB–5 uses the 4–pin solution.

Alert Signal Generation

A buzzer is used for giving alerting tones and/or melodies as a signal of an incoming call. Also keypress and user function response beeps are generated with the buzzer. The buzzer is controlled with a BuzzerPWM output signal from the MAD2WD1. A dynamic type of buzzer is used since the supply voltage available cannot produce the required sound pressure for a piezo type buzzer. The low impedance buzzer is connected to an output transistor that gets drive current from the PWM output. The alert volume can be adjusted either by changing the pulse width causing the level to change or by changing the frequency to utilize the resonance frequency range of the buzzer.

Digital Control

MAD2WD1

The baseband functions are controlled by the MAD2WD1 ASIC, which consists of a MCU, a system ASIC, and a DSP. The GSM/PCN-specific ASIC is named MAD2. There are separate controller ASICs in TDMA and JDC named MAD1 and MAD3. All the MAD2WD1 ASICs contain the same core processors and similar building blocks, but differ from each other in system specific functions, pinout, and package types.

- MAD2WD1 contains following building blocks:
  - ARM RISC processor with both 16–bit instruction set (THUMB mode) and 32–bit instruction set (ARM mode)
  - TMS320C542 DSP core with peripherials:
    – API (Arm Port Interface memory) for MCU–DSP communication,

DSP code download, MCU interrupt handling vectors (in DSP RAM) and DSP booting
– Serial port (connection to PCM)
– Timer
– DSP memory

- BUSC (BusController for controlling accesses from ARM to API, System Logic, and MCU external memories, both 8– and 16–bit memories)

- System Logic
  – CTSI (Clock, Timing, Sleep and Interrupt control)
  – MCUIF (Interface to ARM via BUSC). Contains MCU BootROM
  – DSPIF (Interface to DSP)
  – MFI (Interface to COBBA_GJP AD/DA Converters)
  – CODER (Block encoding/decoding and A51&A52 ciphering)
  – AccIF (Accessory Interface)
  – SCU (Synthesizer Control Unit for controlling 2 separate synthesizer)
  – UIF (Keyboard interface, serial control interface for COBBA_ GJP PCM Codec, LCD Driver, and CCONT)
  – UIF+ (roller/ slide handling)
  – SIMI (SimCard interface with enhanced features)
  – PUP (Parallel IO, USART and PWM control unit for vibra and buzzer)
  – FLEXPOOL (DAS00308 FlexPool Specification)
  – SERRFI (DAS00348 COBBA_GJP Specifications)

The MAD2WD1 operates from a 13 MHz system clock, which is generated from the 13Mhz VCXO frequency. The MAD2WD1 supplies a 6.5MHz or a 13MHz internal clock for the MCU and system logic blocks and a 13MHz clock for the DSP, where it is multiplied to 78 MHz DSP clock. The system clock can be stopped for a system sleep mode by disabling the VCXO supply power from the CCONT regulator output. The CCONT provides a 32kHz sleep clock for internal use and to the MAD2WD1, which is used for the sleep mode timing. The sleep clock is active when there is a battery voltage available; i.e., always when the battery is connected.

MAD2WD1 pinout

MAD2WD1 pins and their usage are described in the following table.

Table 10: MAD2WD1 pin list

Ball No.	Pin Name	Pin Type	Drive / pull	Description	HD955 Function
A1	MCUGenIO0	I/O	2	MCU general purpose I/O	DLR-3 (data cable) power control bit
B1	SynthClk	O	2		Synth clk control bit to SUMMA

C1	DSPGenOut2	I/O	2	DSP general purpose port	TXL to RF
D1	LCDCSX	I/O	2	Serial LCD chip select – external pull-up/down	LCDEN
E1	LEADVCC0	PWR		LEAD power	Supply = VBB
F1	Row0	I/O	2/up	Keyboard row0, parallel LCD driver data	Keyboard row0
G1	VCC_CORE	PWR		Power supply for core	Supply = V2V
H1	VCC_IO	PWR		I/O power supply	Supply = VBB
J1	MCUAd16	O	2	MCU address bus	SRAM/FLASH address 16
K1	MCUAd13	I/O	2	MCU address bus	SRAM/FLASH address 13
L1	ARMGND			ARM GND	GND
M1	MCUAd6	I/O	2	MCU address bus	SRAM/FLASH address 6
N1	MCUAd2	I/O	2	MCU address bus	SRAM/FLASH address 2
A2	TxPA	I/O	2/down	Power amplifier control	TXP to RF
B2	SynthData	O	2	Synthesizer data	SDATA to SUMMA
C2	LEADGND			LEAD gnd	GND
D2	Col4	I/O	2/up	Keyboard column 4 – programmable pull-up	Keyboard col4
E2	Row4	I/O	2/up	Keyboard row 4, parallel LCD dirver register selection control	Keyboard row4
F2	Row1	I/O	2/up	Keyboard row 3, parallel LCD driver data	Keyboard row1
G2	MCUAd21	I/O	2/up	MCU address bus	FLASH address 21
H2	MCUAd18	O	2	MCU address bus	SRAM/FLASH address 18
J2	MCUAd15	I/O	2	MCU address bus	SRAM/FLASH address 15
K2	MCUAd12	I/O	2	MCU address bus	SRAM/FLASH address 12
L2	MCUAd9	I/O	2	MCU address bus	SRAM/FLASH address 9
M2	MCUAd8	I/O	2	MCU address bus	SRAM/FLASH address 8
N2	MCUAd1	I/O	2	MCU address bus	SRAM/FLASH address 1
A3	FrACtrl	I/O	2/down	RF front amplifier control	LNA_AGC
B3	SynthEna1X	O	2	Synthesizer1 data enable	Synth enable (SUMMA)
C3	Col0	I/O	2/up	Keyboard column 0	Keyboard column 0
D3	Col3	I/O	2/up	Keyboard column 3	Keyboard column 3

E3	Row5LCDCD	I/O	2/up	Keyboard row5 data I/O, serial LCD driver command/ data indicator, parallel LCD driver read/write select	LCDCD (LCD driver command/data indicator)
F3	Row2	I/O	2/up	Keyboard row2, parallel LCD driver data	Keyboard row2
G3	MCUAd20	I/O	2/down	MCU address bus	SRAM/FLASH address 20
H3	MCUAd17	O	2	MCU address bus	SRAM/FLASH address 17
J3	MCUAd14	I/O	2	MCU address bus	SRAM/FLASH address 14
K3	MCUAd11	I/O	2	MCU address bus	SRAM/FLASH address 11
L3	MCUAd8	I/O	2	MCU address bus	SRAM/FLASH address 8
M3	MCUAd4	I/O	2	MCU address bus	SRAM/FLASH address 4
N3	MCUAd0	O	2	MCU address bus	SRAM address 0
A4	DSPGenOut4	I/O	2	DSP general purpose port	IRON – Enable control for IrDa
B4	SynthEna2X	I/O	2	Synthesizer 2 data enable	NC
C4	Col1	I/O	2/up	Keyboard column 1	Keyboard column 1
D4	Col2	I/O	2/up	Keyboard column 2	Keyboard column 2
E4	GND	GND		Ground	GND
F4	Row3	I/O	2/up	Keyboard row3, parallel LCD driver data	Keyboard row3
G4	MCUAd19	O	2	MCU address bus	SRAM/FLASH address 19
H4	LEADGND	GND		LEAD ground	GND
J4	GND	GND		Ground	GND
K4	ARMVCC	PWR		ARM power	VBB
L4	MCUAd7	I/O	2	MCU address bus	SRAM/FLASH address 7
M4	MCUAd3	I/O	2	MCU address bus	SRAM/FLASH address 3
N4	VCC_CORE	PWR		Core power	Core power – supplied from CCONT V2V
A5	DSPGenOut5	O	2	DSP general purpose output, COBBA reset	COBBA reset
B5	MBUS	I/O	2/up	MBUS, Flash clock – external pull-up	MBUS, Flash clock
C5	AccTxData	O	2	Accessory Tx data, Flash_Tx – external pull-up	Accessory Tx data, Flash_Tx (FBUS_Tx)
D5	GND	GND		Ground	GND
K5	MCUAd10	O	2	MCU address bus	SRAM/FLASH address 10
L5	GND	GND		Ground	GND

M5	MCURdX	O	2	MCU read strobe	MCU read strobe – OE to memories
N5	MCUWrX	O	2	MCU write strobe	MCU write strobe – WE to memories
A6	COBBACSX	O	2	Chip select for COBBA	COBBA chip select
B6	VCC_IO	PWR		I/O power	VBB
C6	COBBAClk	O	4	COBBA clock, 13MHz	COBBA clk (RFIclk)
D6	AccRxData	I		Accessory Rx data, Flash_Rx	Accessory Rx data, Flash_Rx (FBUS_Rx)
K6	ExtMCUDa0	I/O	2/down	MCU data bus	SRAM/FLASH data 0
L6	ExtMCUDa1	I/O	2/down	MCU data bus	SRAM/FLASH data 1
M6	ExtMCUDa2	I/O	2/down	MCU data bus	SRAM/FLASH data 2
N6	ExtMCUDa3	I/O	2/down	MCU data bus	SRAM/FLASH data 3
A7	COBBASDa	I/O	2	Transfer of control data	Transfer of control data (COBBA SD)
B7	VCC_CORE	PWR		Core power	Core power – supplied from CCONT V2V
C7	COBBAIDa	I/O	2	Bidirectional transfer of in-phase samples	Bidirectional transfer of in-phase samples (COBBA Idata)
D7	COBBAQDa	I/O	2	Bidirectional transfer of quadrature samples	Bidirectional transfer of quadrature samples (COBBA Qdata)
K7	VCC_IO	PWR		I/O power	VBB
L7	ExtMCUDa4	I/O	2/down	MCU data bus	SRAM/FLASH data 4
M7	ExtMCUDa5	I/O	2/down	MCU data bus	SRAM/FLASH data 5
N7	ExtMCUDa6	I/O	2/down	MCU data bus	SRAM/FLASH data 6
A8	PCMSClk	I/O	Down	Transmit frame sync, FSX	Transmit frame sync, FSX (to COBBA)
B8	PCMDClk	I/O	Down	Transmit clock, CLKX	Transmit clock, CLKX (to COBBA)
C8	PCMIO	I/O			ROLLER_A – Input bit for roller
D8	DSPXF	I/O	2/up	External flag	External flag – NC
K8	MCUGenIODa2	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 10
L8	MCUGenIODa1	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 9
M8	MCUGenIODa0	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 8

N8	ExtMCUDa7	I/O	2/down	MCU data bus	SRAM/FLASH data 7
A9	PCMRxData	I/O	Up	Receive data, Rx	Receive data, Rx (from COBBA PCMTx)
B9	PCMTxData	I/O	2/down	Transmit data, Tx	Transmit data, Tx (to COBBA PCMRx)
C9	GND	GND		Ground	GND
D9	BuzzPWM	I/O	2/down	Buzzer PWM control	Buzzer PWM control
K9	GND	I/O		Ground	GND
L9	MCUGenIODa5	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 13
M9	MCUGenIODa4	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 12
N9	MCUGenIODa3	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 11
A10	GenSCIk	O	2	Serial clock	Serial clock (to LCD)
B10	GenSDIO	I/O	2	Serial data in/out – external pull-up/down depending on how to boot	Serial data in/out (to LCD)
C10	GenCCONTCSX	O	2	Chip select to CCONT	Chip select to CCONT
D10	VCC_IO	PWR		I/O Power	I/O Power (VBB)
E10	GND	GND		Ground	GND
F10	HeadDet	I/O		Headset detection interrupt	Headset detection interrupt (to CCONT EAD)
G10	MCUGenIO4	I/O	2	MCU data in 16-bit mode pullup	BATTIO through BTEMP
H10	LEADVCC	PWR		LEAD power	LEAD pwr (VBB)
J10	SCGND	GND		Special cell ground	GND
K10	SCVCC	PWR		Special cell power	VBB
L10	MCUGenIODa7	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 15
M10	VCC_CORE	PWR		Core power	Core power – supplied from CCONT V2V
N10	MCUGenIODa6	I/O	2/down	General purpose I/O port – MCU data in 16-bit mode	FLASH data 14
A11	SIMCardIOC	O	2	SIM data in/out control	SIM data in/out control (to CCONT)
B11	SIMCardRstX	O	2	SIM reset	SIM reset (to CCONT)
C11	SIMCardData	I/O	2	SIM data	SIM data (to CCONT)
D11	LEADVCC	PWR		LEAD power	LEAD pwr (VBB)

E11	VCXOPwr	O	2	VCXO regulator control	Sleep control (to CCONT SLEEPX input)
F11	HookDet	I/O		Non-MBUS accessory connection detector	Non-MBUS accessory connection detector (system conn. XEAR)
G11	VCC_CORE	PWR		Core power	Core power – supplied from CCONT V2V
H11	MCUGenIO1	I/O	2/up	General purpose I/O port	FLASH write protect
J11	ROM2SelX	I/O	2/up	Extra chip select, can be used as MCU general output	Enable for 2M FLASH chip
K11	RFClk	I		System clock from VCTCXO	System clock from VCTCXO
L11	JTDO	I/O	2/up	JTAG data out	JTAG data out
M11	RAMSelX	O	2	RAM chip select	RAM chip select
N11	ROM1SelX	O	2	ROM chip select	Enable for 4M FLASH chip
A12	SIMCardClk	O	2	SIM clock	SIM clock (to CCONT)
B12	CCONTInt	I		CCONT interrupt	CCONT interrupt
C12	TxPwr	I/O	2/down	Tx regulator control	Tx regulator control (to CCONT)
D12	SIMCardPwr	I/O	2/up	SIM power control	SIM power control (to CCONT)
E12	MCUGenIO3	I/O	2/up	General purpose I/O port	VPP supply for FLASH
F12	LoByteSelX	I/O	2/up		ROLLER_B – Input bit for roller
G12	VibraPWM	I/O	2/down	Vibra PWM control	Vibra PWM control
H12	TestMode	I	Down	Test mode select	Test mode select (GND)
J12	GND	GND		Ground	GND
K12	RFClkGnd	I		System clock reference ground input	System clock reference ground input (GND)
L12	CoEmu0	I/O	2/up	DSP/MCU emulation port 0	DSP/MCU emulation port 0 – JTAG
M12	JTClk	I/O	Up	JTAG clock	JTAG clock
N12	JTRst	I/O	Down	JTAG reset	JTAG reset
A13	Clk32k	I		Sleep clock oscillator input	Sleep clock oscillator input
B13	PURX	I		Power-up reset	Power-up reset (from CCONT)

C13	RxPwr	I/O	2/down	Rx regulator control	Base tune enable/disable control
D13	SynthPwr	I/O	2/down	Synthesizer regulator control	Transmit power control enable
E13	MCUGenIO2	I/O	2/up	General purpose I/O port	LCDRSTX – LCD reset control
F13	LEADGND	GND		LEAD ground	GND
G13	VCC_IO	PWR		VCC power	VBB
H13	ExtSysResetX	O	2	System reset	FLASH read protect control
J13	EEPROMSelX	I/O	2/up	EEPROM chip select, can be used as MCU gernal output	ROLLER_C – input bit for roller
K13	SIMCardDetX	I		SIM card detection	SIM card detection (to CCONT BSI input)
L13	CoEmu1	I/O	2/up	DSP/MCU emulation port 1	DSP/MCU emulation port 1
M13	JTMS	I/O	Up	JTAG mode select	JTAG mode select
N13	JTDI	I/O	Up	JTAG data in	JTAG data in

Table 11: COBBA_GJP pin list

Ball No.	Name	Type	Reset Value	Description	HD955 Function/Connection
A1	MIC1P	I	-	Positive high impedance input for microphone	Analog input from external microphone
B1	MIC3N	I	-	Third negative high impedance input for microphone	Analog input from external microphone
C1	VSUBA	P		Analog Substrate contact for RF analog and AudioCodec	AGND
D1	EARP	O	Float	Positive ear-piece output	To internal speaker
E1	HF	O	Float	Output for phone external audio circuitry	To system connector for external analog audio
F1	VDA2	P	-	Positive analog power supply for the transmitters	VCOBBA from CCONT
G1	IREF	O	float	Reference current output (no capacitance allowed on this pin)	Through 100k to AGND
H1	VSA2	P	-	Negative analog power supply for the tranmitters	AGND
A2	MIC1N	I	Inp	Negative high impedance input for microphone	Analog input from external microphone
B2	MIC3P	I	-	Third positive high impedance input for microphone	Analog input from external microphone

C2	VSA5	P	-	Negative analog power supply for PCM ADC	AGND
D2	EARN	O	Float	Negative ear-piece output	To internal speaker
E2	VSA4	P	-	Negative analog power supply for PCM DAC	AGND
F2	VREF	I	-	Reference voltage input (1.5V)	VREF from CCONT
G2	AFCOut	O	Float	Automatic frequency control output	To 13MHz clock oscillator
H2	TxIOutN	O	Float	Negative in-phase transmit output	To SUMMA
A3	MIC2N	I	Inp	Second negative high impedance input for microphone	Analog input from slide microphone
B3	MIC2P	I	Inp	Second positive high impedance input for microphone	Analog input from slide microphone
C3	VDA5	P	_	Positive analog power supply for PCM ADC	VCOBBA from CCONT
D3	HFCM	O	Float	Common mode output for phone external audio circuitry	Not used (floating)
E3	VDA4	P	-	Positive analog power supply for PCM DAC	VCOBBA from CCONT
F3	TxQOutP	O	Float	Positive quadrature transmit output	To SUMMA
G3	TxQOutN	O	Float	Negative quadrature transmit output	To SUMMA
H3	TxIOutP	O	Float	Positive in-phase transmit output	To SUMMA
A4	MBIAS	O	Float	Bias output for microphone 2.1V	Bias output for microphone 2.1V
B4	VDD1	P	-	AudioCodec positive digital power supply	VBB
C4	VSS1	P	-	AudioCodec negative digital power supply	GND
D4	AUXOUT	O	Float	Auxiliary audio output or ABIAS 2.1V	Auxiliary audio output or ABIAS 2.1V
E4	VDA3	P	-	Positive analog power supply	VCOBBA from CCONT
F4	TxCOut	O	Float	Transmit power control output	Transmit power control output – to SUMMA
G4	TxIPhsP	O	Float	Positive in-phase PHS transmit output	Not used (floating)
H4	TxIPhsN	O	Float	Negative in-phase PHS transmit output	Not used (floating)
A5	TEST	I	Inp	Test pin	GND

B5	PCMTx	I/O	‘Z’	PCM bus receive data (4-wire) / I/O data (1-wire)	To MAD2WD1 PCMRxData
C5	PCMSCLK	O	‘Z’	8 kHz frame sync (4-wire) / Pdata(8) (1-wire)	To MAD2WD1 PCMSClk
D5	PCMRx	I/O	‘Z”	PCM bus receive data (4-wire) / Pdata(10) (1-wire)	To MAD2WD1 PCMTxData
E5	Pdata(0)	O	‘0’	Pdata(0) / Scanselect when test=1	Not used (floating)
F5	AGCOut	O	0V	Second output of TxC DAC – Rx gain control voltage	To SUMMA
G5	TxQPhsP	O	Float	Positive quadrature PHS transmit output	Not used (floating)
H5	TxQPhsN	O	Float	Negative quadrature PHS transmit output	Not used (floating)
A6	Idata	I/O	Inp	Bi-directional transfer of I-samples / Pdata(5) when JDC+IQ=0 and DuplexIQ=0 and JDC mode	To MAD2WD1 COBBAIda
B6	Qdata	I/O	Imp	Bi-directional transfer of Q-samples / Pdata(6) when JDC+IQ=0 and DuplexIQ=0 and JDC mode	To MAD2WD1 COBBAQda
C6	PCMDCLK	O	‘Z’	PCM bus data transfer clock (4-wire) / Pdata(9) (1-wire) – 520 kHz	To MAD2WD1 PCMDClk
D6	Pdata(3)	O	‘0’	Pdata(3) / RxI data in DuplexIQ mode	LCD light (LED) driver control
E6	Pdata(1)	O	‘0’	Pdata(1) / Capture/shift when test=1	Keyboard light (LED) driver control
F6	VSA1	P	-	Negative analog power supply for receivers	AGND
G6	AuxDAC	O	0V	Third output of TxC DAC	Not used (floating)
H6	VSA3	P	-	Negative analog power supply	AGND
A7	SD	I/O	Inp	Serial data for the general interface	To MAD2WD1 COBBASDa
B7	CSX	I	Inp	Serial port chip select	To MAD2WD1 COBBACSX
C7	PData(4)	O	‘0’	Pdata(4) / RxQ data in DuplexIQ mode	To CHAPS VLIM (CHAPS output voltage limit)
D7	RFIDAX	O	‘0’	Data available strobe for JDC when JDC+IQ=0 / Pdata(7) otherwise	Not used (floating)
E7	Pdata(2)	O	‘0’	Pdata(2)	PD2 (Switch for 2.1V AUXOUT bias or ABIAS)

F7	RxQN	I	-	Negative Q receive input in Rx_In-phase mode	AGND
G7	VDA1	P	-	Positive analog power supply for the receivers	VCOBBA from CCONT
H7	RxRef	O	Float	Rx path internal reference buffered output	Not used (floating)
A8	VSUB	P	-	Substrate contact for digital logic	GND
B8	VSS2	P	-	RF interface negative digital power supply	GND
C8	VDD2	P	-	RF interface positive digital power supply	VBB
D8	RFIClk	I	Inp	System clock input (13 MHz)	COBBAClk output from MAD2WD1
E8	ResetX	I	Inp	Master system reset	DSPGenOut5 from MAD2WD1
F8	RxQP	I	-	Positive Q receive input in Rx_In-phase mode	AGND
G8	RxIP	I	-	Positive I/common receive input	From SUMMA
H8	RxIN	I	-	Negative I/common receive input	From SUMMA

Table 12: CCONT 3V pin assignment

Pin	Symbol	Type	State in Reset	Description
1	RSSI	I		receive signal strength indicator
2	ICHAR	I		V(ICHAR) voltage input
3	MODE_SEL	I	High Z/GND	mode select High Z=normal mode GND=RAM_Bck
4	VR3/RAM_bck	O	OV/2.8V	VR3 regulator output/RAM backup
5	CNTVR3	I	High Z	Control VR3 regulator
6	CNTVR2	I	High Z	Control VR2 regulator
7	CNTVR5	I	High Z	Control VR5 regulator
8	VBAT	P		unregulated supply voltage (RF)
9	VR2	O	High Z	VR2 regulator output
10	GROUND	P		(RF)
11	VR5	O	High Z	VR5 regulator output
12	VBAT	P		unregulated supply voltage (RF)
13	VREF	O	1.244/1.5V	reference voltage output
14	GROUND	P		(RF)
15	VR4	O	High Z	VR4 regulator output

Table 12: CCONT 3V pin assignment

Pin	Symbol	Type	State in Reset	Description
16	VBAT	P		unregulated supply voltage (RF)
17	CNTVR4	I	High Z	Control VR4 regulator
18	TXPWR	I	High Z	Control VR7 regulator (CNTVR7)
19	VR7BASE	O	High Z	VR7 regulator base current
20	VR7	O	High Z	VR7 regulator output
21	VBAT	P		unregulated supply voltage (RF)
22	VR6	O	2.8V	VR6 regulator output (COBBA_GJP)
23	GROUND	P		(RF)
24	SLEEPX	I	“1”	Control VR1 regulator (CNTVR1)
25	VR1	O	2.8V	VR1 regulator output (VCXO)
26	VR1_sw	O	High Z	VR1 switched output
27	VBAT	P		unregulated supply voltage (RF)
28	VBAT2	P		unregulated supply voltage (VSIM, V5V, SMR, SIMIf)
29	PWRONX/WDDISX	I	VBAT/GND	power on control from keyboard watchdog disable
30	SIM_PWR	I	“1”/”0”	SIM regulator enable
31	GROUND	P		(VSIM, V5V, SMR, SIMIf)
32	V5V	O	High Z	5V dc voltage output
33	V5V_2	O	High Z	reserved for 5V SMR
34	V5V_4	O	High Z	reserved for 5V SMR
35	V5V_3	O	High Z	reserved for 5V SMR
36	VSIM	O	3.0V/High Z	SIM regulator output
37	GROUND	P		(VSIM, V5V, SMR, SIMIf)
38	SIMCLK_O	O	“0”	clock output from SIM interface (5MHz)
39	SIM I/O_C	I	High Z	SIM data I/O control
40	SIMRST_A	I	High Z	SIM interface reset (from MAD2WD1)
41	SIMCLK	I	High Z	clock to SIM interface (5MHz)
42	SIMRST_O	O	“0”	reset output from SIM-interface (to SIM)
43	DATA_O	I/O	“0”	SIM data I/O line
44	DATA_A	I/O	“0”	SIM-interface MAD2WD1 data

Table 12: CCONT 3V pin assignment

Pin	Symbol	Type	State in Reset	Description
45	VBACK	P	backup battery	backup battery input
46	CRA	I		crystal for 32 kHz sleep clock
47	CRB	I		crystal for 32 kHz sleep clock
48	SLCLK	O		sleep clock output
49	DATACLK	I	High Z	MAD2WD1 bus clock
50	DATASELX	I	High Z	MAD2WD1 bus enable
51	DATA_IN/OUT	I/O	High Z	MAD2WD1 bus serial data
52	CCONTINT	O	“0”	CCONT interrupt output
53	TEST	I	GND	test pin (ground=>normal operation)
54	PURX	O	“0”	power up reset signal
55	VBB	O	2.8V	baseband regulator output
56	PWMOUT	O	“0”	PWM out (3/0V)
57	VBAT	P		unregulated supply voltage (VBB, V2V, ADC, 32kHz)
58	GROUND	P		(VBB, V2V, ADC, 32kHz)
59	V2V	O	1.975V	MAD2WD1 core regulator output
60	VCHAR	I		charger voltage
61	VCXOTEMP	I		VCXO-temperature
62	BSI	I		battery type input
63	BTEMP	I		battery temperature input
64	EAD	I		external accessory detection

Memories

The MCU program code resides in an external program memory, size is 16Mbits. MCU work (data) memory size is 1Mbits. A special block in the flash is used for storing the system and tuning parameters, user settings and selections, a scratch pad, and a short code memory.

Separate EEPROM memories formerly used to store non-volatile data have been removed and replaced by dedicated, write-protected blocks in flash memory. This flash solution gives a cost and size benefit in products where large EEPROM sizes are required.

The BusController (BUSC) section in the MAD2WD1 decodes the chip select signals for the external memory devices and the system logic. BUSC controls internal and external bus drivers and multiplexers connected to the MCU data bus. The MCU address space is divided into access areas with separate chip select signals. BUSC supports a programma-

ble number of wait states for each memory range.

Program Memory 32MBit Flash

The MCU program code resides in the flash program memory.

The flash memory has a power down pin that shall be kept low, during the power up phase of the flash to ensure that the device is powered up in the correct state (read only). The power down pin is utilized in the system sleep mode by connecting the VCXOPwr to the flash power down pin to minimize the flash power consumption during the sleep.

SRAM Memory

The work memory size is 4Mbits (512kx8) static ram in a shrinked TSOP–32 package. Vcc is 2.8V and access time is 85 ns The work memory is supplied from the common base-band VBB voltage and the memory contents are lost when the baseband voltage is switched off. All retainable data should be stored into the flash memory when the phone is powered down.

EEPROM Emulated in FLASH Memory

A block in flash is used for a nonvolatile data memory to store the tuning parameters and phone setup information. The short code memory for storing user defined information is also implemented in the flash. The flash size can vary between 2k to 8kbytes depending on the amount of short code number locations supported. The memory is accessed through the parallel bus.

MCU Memory Requirements

The MCU memory requirements are shown below.

Table 13: HD955 memory requirements

Product	Device	Organization	Access Time ns	Wait States Used	Remarks
DCT3.5	FLASH	2Mx16	100	1	32Mbit flash chip, 2.8V read/write
DCT3.5	FLASH	1Mx16	100	1	16Mbit flash chip, 2.8V read/write
DCT3.5	SRAM	512Kx8	85	1	120ns @ 2.8V read/write

Flash Programming

The system connector can be used as a flash prom programming interface for flash memories for updating (i.e. re–programming) the flash program memory. Used system connector pins and their functions are listed in Table 14.

To flash the phone use service battery (BBD–3) this will automatically power up the phone via BTEMP. When flashing, the phone has to be initialized after each file has been flashed. The flash prommer controls the power up of the phone via the service battery.

The program execution starts from the BOOT ROM and the MCU investigates in the early start–up sequence if the flash prommer is connected. This is done by checking the status of the MBUS–line. Normally this line is high, but when the flash prommer is connected, the line is forced low by the prommer. The flash prommer serial data receive line is in receive mode waiting for an acknowledgement from the phone.

The data transmit line from the baseband to the prommer is initially high. When the baseband has recognized the flash prommer, the FBUS TX–line is pulled low. This acknowledgement is used to start the data transfer of the first two bytes from the flash prommer to the baseband on the FBUS RX–line. The data transmission begins by starting the serial transmission clock (MBUS–line) at the prommer.

The 2.8V programming voltage is supplied inside the transceiver from the CCONT.

For protecting the MAD2WD1 against ESD spikes at the system connector, the data transmission lines (MBUS, RX and TX) are equipped with EMI filters.

Table 14: Flash programming, DC connector

Pin	Name	Parameter	Min	Typ	Max	Unit	Remarks
1	VIN	supply voltage	6.8	7.8	8.8	V	supply voltage
2	GND	GND	0		0	V	supply ground
11	MBUS	serial clock from the prommer	2.0 0		2.8 0.8	V	prommer detection and serial clock for synchronous communication
12	FBUS_RX	serial data from the prommer	2.0v 0v		2.8 0.8	V	receive data from prommer to baseband
13	FBUS_TX	data acknowledge to the prommer	2.0 0.1		2.8 0.8	V	transmit data from baseband to prommer
14	GND	GND	0		0	V	supply ground

IBI Accessories

All accessories which can be connected between the transceiver and the battery or which itself contain the battery, are called IBI accessories.

Either the phone or the IBI accessory can turn the other on, but both possibilities are not allowed in the same accessory.

Phone Power–on by IBI

IBI accessory can power on the phone by pulling the BTEMP line up to 3V.

IBI power–on by phone

Phone can power the IBI accessory on by pulling the BTEMP line up by MCUGenIO4 of MAD2. BTEMP measurement is not possible during this time.

The accessory is commanded back to power–off by MBUS message.

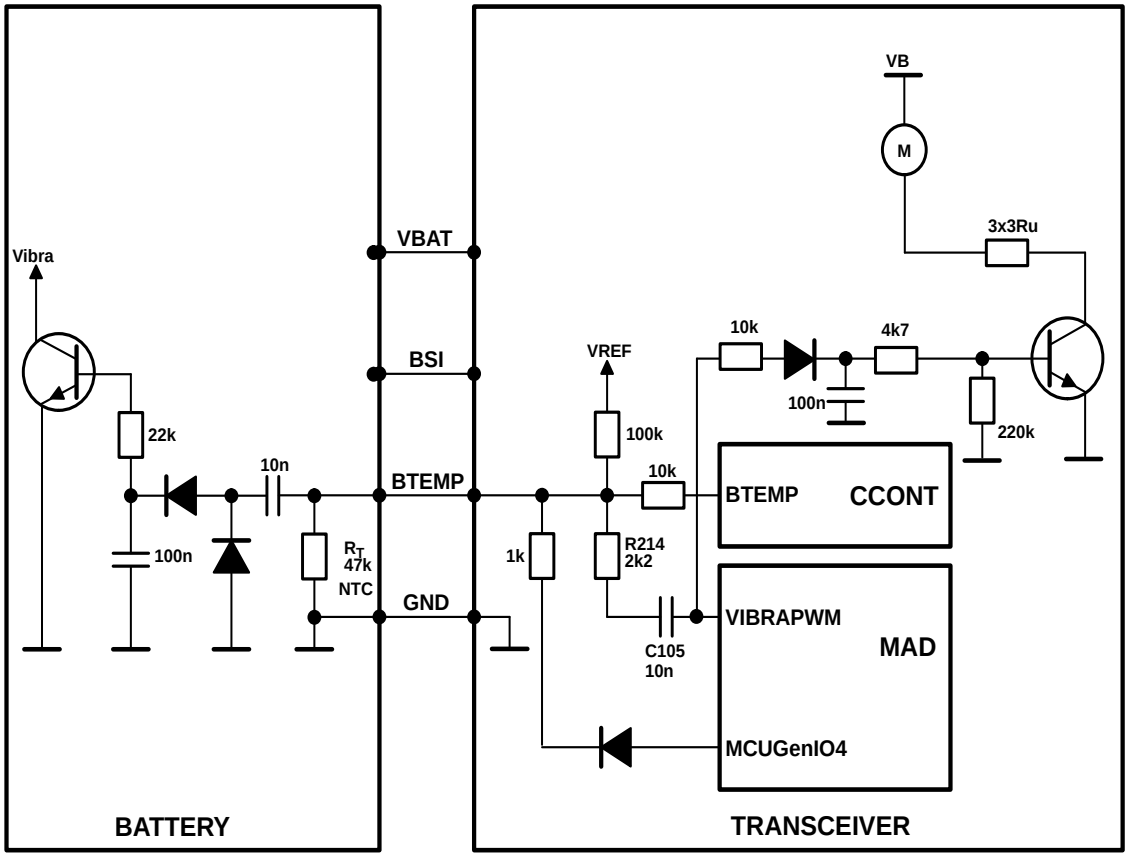


Figure 14: IBI power on

RF Module

RF Frequency Plan

The following figure shows the RF frequency plan used by GSM1900.

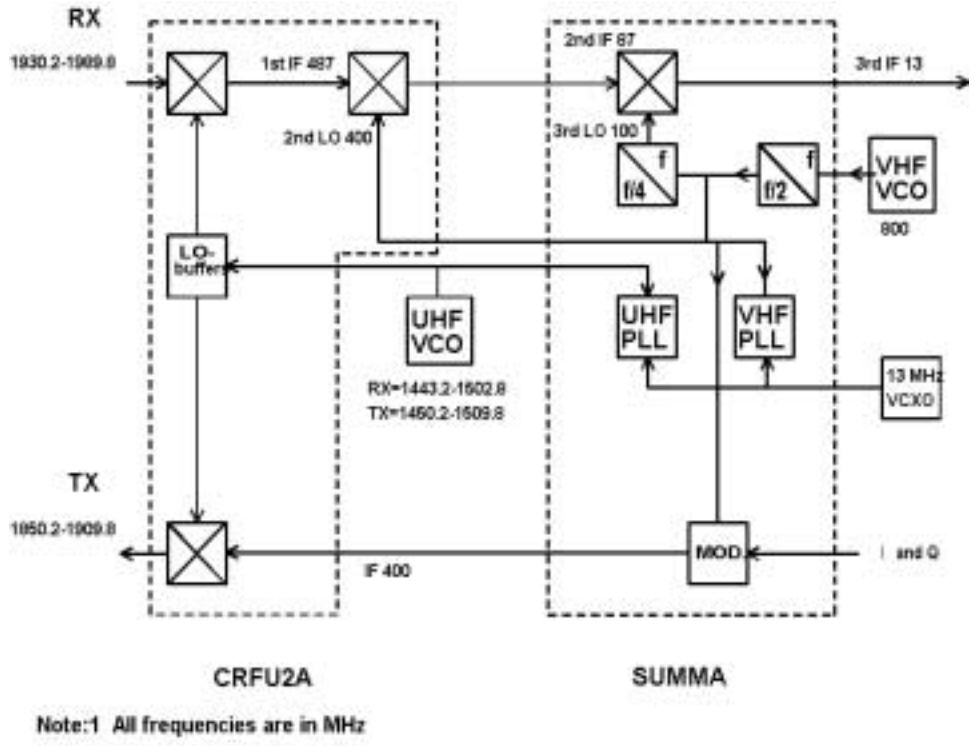


Figure 15: RF frequency plan

DC Characteristics

Power Distribution Diagram

Current consumption of each regulator is shown in the following power distribution diagram (Figure 16 shows maximum currents, Figure 17 shows typical currents). On the left side of the figure, are the regulator control signals. Above each regulator is the rated current for that regulator. The name on the right side of the regulator block (smaller font) indicates the signal name used on the schematics. On the far right side of the figure are the pin names (power) for the different ICs.

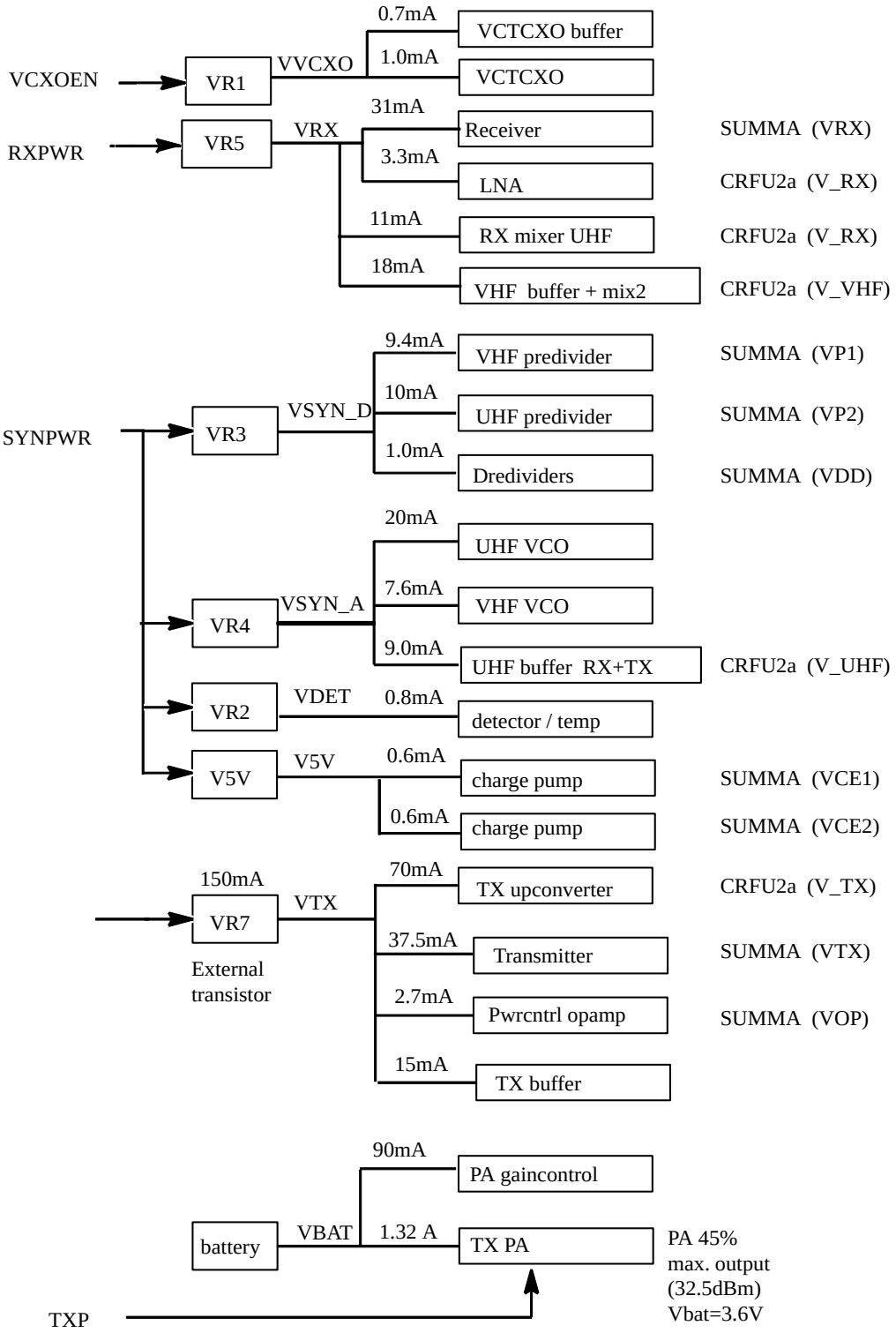


Figure 16: RF power distribution: maximum currents

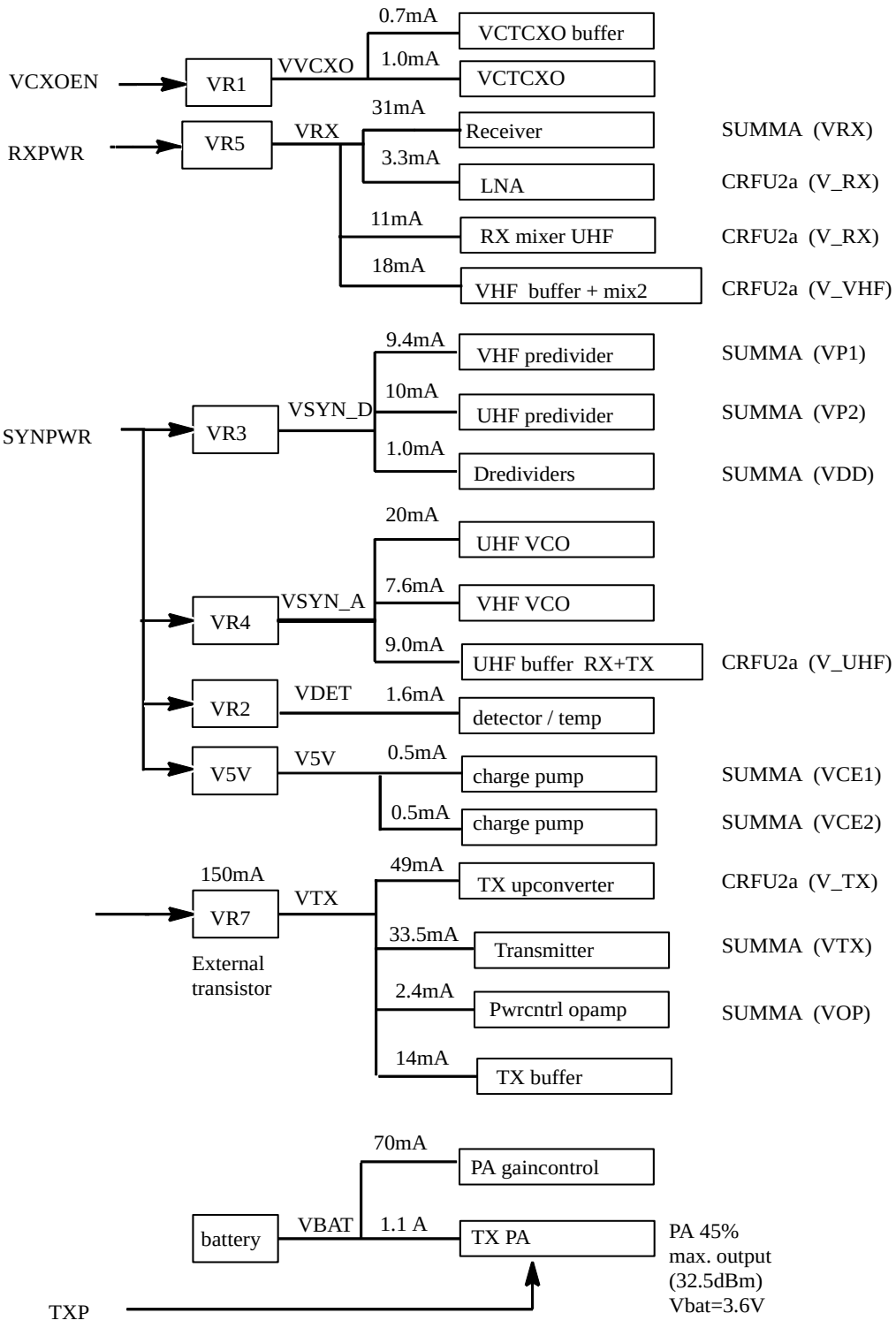


Figure 17: RF power distribution: typical currents

Control Signals

Table 15: Control signals and maximum current consumption

VCXOEN	SYNPWR	RXPWR	TXPWR	TXP	CURRENT consump. (typ.)	CURRENT consump. (max)	Notes
L	L	L	L	L	<10µA	<10µA	leakage current (PA)
H	L	L	L	L	1.7mA	3.0 mA	VCTCXO active
H	H	L	L	L	42.5 mA	61.2 mA	VCTCXO, VCOs PLL active
H	H	H	L	L	107.8 mA	143.8 mA	RX active
H	H	L	H	L	140 mA	186.4 mA	TX active except PA
H	H	L	H	H	1310 mA	1576 mA	TX active full power

Regulator Specifications

Table 16: Current output capability/nominal voltage of RF regulators

Regulator	Maximum output current	Unit	Vout	Unit	Notes
VR1 to VR5	100	mA	2.8	V	
VR7	150	mA	2.8	V	Depends on external BJT
VR7BASE	-10	mA			Base current limit *
V5V	30	mA	5.0	V	

** default power element is PNP BJT. If a FET-device is used, special care must be taken to ensure stability.*

NOTE: Maximum total current from all regulators is 330 mA rms.

Table 17: RF regulator specifications

Characteristics	Condition	Min	Typ	Max	Unit
External compensation capacitor VR1 - VR7	Note: ESR value <<1 ohm Iout=100mA	1	1		µF
External compensation capacitor VR1 - VR7	Note: ESR value <<1 ohm Iout<40mA	0.220	0.220		µF
Output voltage VR1 - VR7	over full temperature, input voltage and load range	2.7	2.8	2.85	V
Tracking error VR1 - VR7	over full temperature, input voltage and load range			tbd (<0.2)	%

Table 17: RF regulator specifications

Characteristics	Condition	Min	Typ	Max	Unit
Line regulation	F v 10kHz	49			dB
Line regulation	F v 100kHz	40			dB
Load regulation	T = 25^0 C		0.6	1	mV/mA
Rise time (1% to 99%), 50mA, depends on load voltage reference/bias already ON, VR1 - VR7	Turn-on	6		70	ms
Overshoot	C = 1µF, turn on/off		3		%
Settling time (to 0.1% of nominal), 50 mA, depends on load, voltage reference/bias already ON	C = 1µF, turn on from CNTVRx rise	6			ms
Phase margin	C = 1µF	45			o
Total noise density			200		nVrms/pHz
Short-circuit current. Note: The chip does not tolerate continuous short-circuit current.	output shorted to ground		250	350	mA
Supply current (each regulator)	ON mode		I_{out}/ 60+330	I_{out}/ 10+540	mA

NOTE 1: Characteristics above are NOT valid if VBAT < 3.0V.

NOTE 2: Line regulation is 20dB for f<100kHz when battery voltage is lower than 3.1V.

NOTE 3: The 220nF can be divided into two capacitors; one as close to CCONT as possible, the other next to the RF parts.

NOTE 4: If the output current is less than 10mA, a 1uF is required to ensure stability.

Functional Description

RF Block Diagram

Refer to |4| which is the RF block diagram in Design Architect format. The related component number is referenced to (..), so it is easier to locate that specific component.

As can been seen from the RF block diagram, most of the functions have been integrated into three ASICs. CRFU_2a (N600) is a wideband UHF ASIC with both receiver and transmitter functions.

The receiver functions include LNA and two downconversion mixers (Gilbert cell) with LO buffers. The transmitter functions include an upconversion mixer (image rejection) with LO buffer. All inputs/outputs are wideband and require external matching networks for

optimal performance.

SUMMA (N700) provides two main functions:
1. RX/TX blocks
2. PLL

The receiver includes a Receive Controlled Gain Amplifier, a mixer with LO buffers and IF amplifiers. The transmitter section includes a Transmit Controlled Gain Amplifier, an I/Q Modulator, circuitry required to generate the Quadrature Local Oscillator and Transmit Power Control which controls the MMIC PA (N500) output power.

The PLL section is control via a serial bus and contains both UHF and VHF PLL and predividers.

The MMIC PA (N500) uses gallium–arsenide heterojunction bipolar transistor (GaAs HBT) technology. The PA has an overall dynamic range of 45dB, and is capable of producing 32.5dBm output power with 0dBm input.

Interfacing with the above ASICs are four more ASICs. These include:
1. CCONT (N100)– is a multifunction power management IC. This ASIC contains six 2.8V linear regulators used in the RF section as well as two 2.8V regulators used in the BB section. CCONT also contains a switch mode supply power which generates +5V which is used to power the charge pumps in SUMMA. Some of the features of this IC are a nine channel A/D converter, power up/down procedures, reset logic, charging control, watch-dog, sleep control, and SIM interface.

2. COBBA_GJP (N300)– is an interface between the digital world of the BB processing and the analog world of RF and audio circuitry.

3. MAD2_PR1 (D200) – contains system logic and DSP

4. CHAPS – charging control ASIC

Receiver

The receiver is a triple conversion receiver consisting of two ASICs; CRFU_2a (N600) and SUMMA (N700). CRFU_2a contains LNA bias circuitry with an external transistor which provides step gain, depending on the incoming RF level and the first and second mixers. SUMMA contains the third mixer. All filtering is external.

The received RF signal from the antenna is fed via the duplex filter (3 pole bandpass filter; Z502) to the LNA. LNA input and output matching networks are external. The LNA gain step is controlled by MAD2_WD1 (FRAC, D200). Gain step in LNA is activated when the receive RF level is below –48 dBm.

Following the LNA, the signal is fed to a 3 pole ceramic bandpass filter (Z602). The combination of the duplex filter and the bandpass filter define the blocking characteristics of the receiver.

The bandpass filtered signal is fed back to CRFU_2a, where the signal is down converted with a double balanced active mixer (Gilbert cell) to 487 MHz. The local oscillator signal for this down conversion is generated by the UHF VCO (G700) and buffered in CRFU_2a. The first IF signal is bandpass filtered with SAW filter, which has external matching networks in both ends. This filter attenuates the intermodulating and image frequencies. The second down conversion (occurs in CRFU_2a) results in a balanced IF of 87 MHz, which is filtered using an 87 MHz SAW filter (Z700). This filter provides selectivity for channels greater than +/– 200 kHz, and attenuates the image frequency of the third mixer and intermodulating signals. The local oscillator signal for this down conversion is 400 MHz, which is generated by the 800 MHz VHF VCO module (G702). The VHF VCO signal is buffered and divided in SUMMA and the 400 MHz resulting signal is again buffered in CFRU2a before the mixer.

After the 87 MHz filter, the signal is fed into the AGC amplifier which has been integrated into SUMMA. The AGC amplifier contains analog gain control which provides accurate gain control (minimum 57 dB) for the receiver. Control voltage for the AGC is generated by the D/A converter in COBBA_GJP (N300). The final mixing stage occurs in SUMMA with a local oscillator signal of 100 MHz generated by dividing the VHF–synthesizer output (800 MHz) by eight.

The third (final) IF filter (Z701) is a ceramic bandpass filter with a center frequency of 13 MHz. This filter attenuates adjacent channels with very little attenuation for +/– 200 kHz. The +/– 200 kHz interferers are filtered digitally by DSP. The 13 MHz bandpass signal is converted to a balanced signal with a buffer circuit in SUMMA. This buffer circuit has a voltage gain of 36 dB. This balanced signal is then fed to COBBA_GJ. The PGA stage in COBBA_GJP has a gain setting of either 0 dB or 9.5 dB, which is controlled via the COBBA_GJP control bus. For HD955 the PGA gain will be set to 0dB.

Transmitter

Transmitter chain consists of IQ–modulator, upconversion mixer, TX filter, TX buffer, and a poweramplifier.

The differential I and Q signals are generated by COBBA_GJP and are filtered by an external RC network (R501, R504, R505, R506, R514, R517, C525 and C526, fc=200kHz) before being fed into the IQ modulator in SUMMA (N700). The modulator generates a TX IF of 400 MHz, which is derived from the VHF synthesizer output (divide by two). Inside SUMMA the 400 MHz is amplified and then fed to an external filter before being upconverted in CRFU_2a. The upconverter in CRFU_2a is a double balanced image rejection mixer. The local oscillator signal for the upconversion is generated by the UHF synthesizer.

After CRFU_2a there is SAW filter (Z503) to attenuate the spurious signals generated in the upconversion mixer in CRFU_2a.

After SAW filter TX–signal is amplified in discrete bufferstage that has 10 dB gain. Following discrete TX–buffer is a 3-pole ceramic bandpass filter (Z603), which attenuates the image frequency, LO leakage, and wideband noise.

After filtering, the signal goes to the final amplifier, which is a MMIC PA (N500) with an input impedance of 50 ohms. The MMIC contains three amplifier stages with interstage matching. The first amplifier stage is variable and is control by the TX power control circuitry. An external driver is required to supply the necessary current to the TX power control circuitry. The PA has over 45 dB power gain and is capable of producing an output of 32.5 dBm with an input of 0 dBm. Harmonics generated by the nonlinear PA (class AB) are attenuated with the output external matching net work and the low-pass/bandstop filtering in the duplexer (Z502).

Power control circuitry consists of a power detector, an error amplifier in SUMMA and the A/D converter in CCONT (N100). The directional coupler is situated between the power amplifier and duplex filter. The power detector is a combination of a directional coupler and a diode rectifier. The directional coupler converts the forward going power with a certain ratio into a signal which is rectified by a schottky diode and a filter to create a DC voltage. This DC voltage is fed to
1. A/D converter in CCONT which holds a sample of the detector output (no RF signal); then MCU/DSP sets the TXC voltage accordingly for the following burst.
2. The error amplifier in SUMMA

The error amplifier in SUMMA compares the detected voltage and the TXC voltage, which is generated by a D/A converter in COBBA_GJ. This creates a closed control loop and since the gain control characteristics of the PA are linear in the absolute scale, the output burst of the PA tracks the TXC voltage linearity.

Power Detection Circuit

The power detector gives an indication of output RF power by rectifying the RF voltage to a DC voltage. Ideally the output voltage of this peak envelope detector is the peak value of the RF voltage but in real world the output voltage is somewhat smaller depending on the quality of the detector diode.

A bias current is driven through the detector diode, which causes an additional voltage component to the output of the detector. The output voltage is then a sum of the rectified voltage and the bias voltage. This bias voltage is a function of biasing resistors, supply voltage and the voltage knee of the diode. At small RF power levels the rectified voltage can be only a few millivolts/dB which means that all other voltage components should remain very stable to achieve a reliable indication of the output power.

However, the variation of the knee voltage of the diode alone causes more than 100 mV variation in the output voltage over the specified temperature range. Furthermore, the temperature variation varies the rectifying sensitivity of the detector diode but this effect is less significant. With a simple passive bias network, the bias current of the diode will also change with temperature and this effect can be used to partially cancel the variation of the sensitivity.

In order to avoid the bias voltage variation ruining the accuracy of the power control loop, the bias voltage of the detector has to be monitored and included in the power control voltage (TXC), which determines the output power. The detector bias voltage monitoring is accomplished by periodically measuring the output voltage of the detector

at a moment when no RF power is being transmitted. This measured voltage is converted into a digital signal by an A/D converter where it is used by DSP as part of the control voltage. Ideally the control voltage is formed as a sum of exactly the same components as the output voltage of the detector, the rectified voltage and the bias voltage. The rectified voltage component sets the output power and should obey the peak envelope sensitivity curve of the detector diode offset with the coupling factor of the directional coupler. The bias voltage is measured and updated in the control voltage often enough so that no remarkable temperature drift has time to occur. The bias voltage must be measured before the first burst of the transmission period. The detector diode is located close to the receiver so that the bias voltage measurement can also be used to indicate the receiver temperature as well if needed (RSSI correction).

The third voltage component affecting the operation of the power control loop in addition to the rectified RF and bias voltages is the offset voltage of the error amplifier. An operational amplifier is integrated in SUMMA and is used as the error amplifier. The input offset voltage should remain relatively stable with temperature but the variation from device to device can be several tens of millivolts.

Therefore the offset voltage must to be taken into account when tuning the power control loop in operation. This means adding or subtracting an offset correction to the power control voltage. A fixed correction will probably suffice, although the input offset voltage is actually dependent on the common mode input voltage of the loop amplifier. The value of the offset correction should then be defined at a low power control voltage where the error due to the offset voltage is the most significant.

The power control voltage has the following formula:

$U_{txc} = U_{rf} + k * U_{bias} + U_{offset}$, where
U_{txc} = power control voltage
U_{rf} = RF output level setting voltage
k = constant
U_{bias} = bias voltage at the output of the detector
U_{offset} = correction voltage due to loop amplifier input offset.

The RF output level setting U_{rf} has values approximately from 20mV to 2V according to the applied power level. The voltages at each power level can be predetermined if the variation between the individual detector diodes is not too large. If the peak envelope sensitivity of the detector varies considerably with temperature a temperature dependent correction must to be added to the value of U_{rf} . An indication of temperature can be obtained from the detector output bias voltage measurement.

The constant coefficient k is needed to compensate the voltage division from the output of the COBBA D/A converter to the input of the loop amplifier. This is due to output/input resistances of the devices. A proper selection of k also reduces the error due to detector peak envelope sensitivity variation with temperature. The value of k is likely to be slightly above 1.

The bias voltage U_{bias} at the output of the detector is measured with an A/D converter

which is sampled so that no transmitter output RF signal is present during the measurement. A settling time of about 1ms should be allowed before the sampling is done after a transmitted burst. The values of the U_{bias} range approximately from 50mV to 200mV.

The loop amplifier input offset correction voltage ranges from –70mV to 70mV. The actual value will be measured for each RF module in production tuning. As this is likely to be a fixed correction it can be included in the stored values of U_{rf} which saves the arithmetics needed to calculate the power control voltage.

If needed, temperature indication can be derived from the value of U_{bias}. A reference voltage $U_{tempref}$ however is needed to calibrate the temperature scale. The reference voltage is the value of U_{bias} measured at a known temperature during production tuning. The accuracy requirement for the temperature measurement won't be particularly high so that the calibration shouldn't call for any special arrangements deviating from the RF tuning procedure. $U_{tempref}$ shall be stored in the phone.

A frequency correction is possibly needed in U_{rf}. This is due to duplex filter attenuation at higher end of the transmitter band and possible frequency slope of the directional coupler coupling factor.

To correct for the first TX slot (after phone is powered up), the bias voltage will be measured by MCU during the IDLE MODE and the TXC value corrected by DSP. Otherwise, the bias voltage will be measured during the IDLE FRAME, with the TXC valued updated in the next multi–frame. This means a worst case delay of approximately 120 msec.

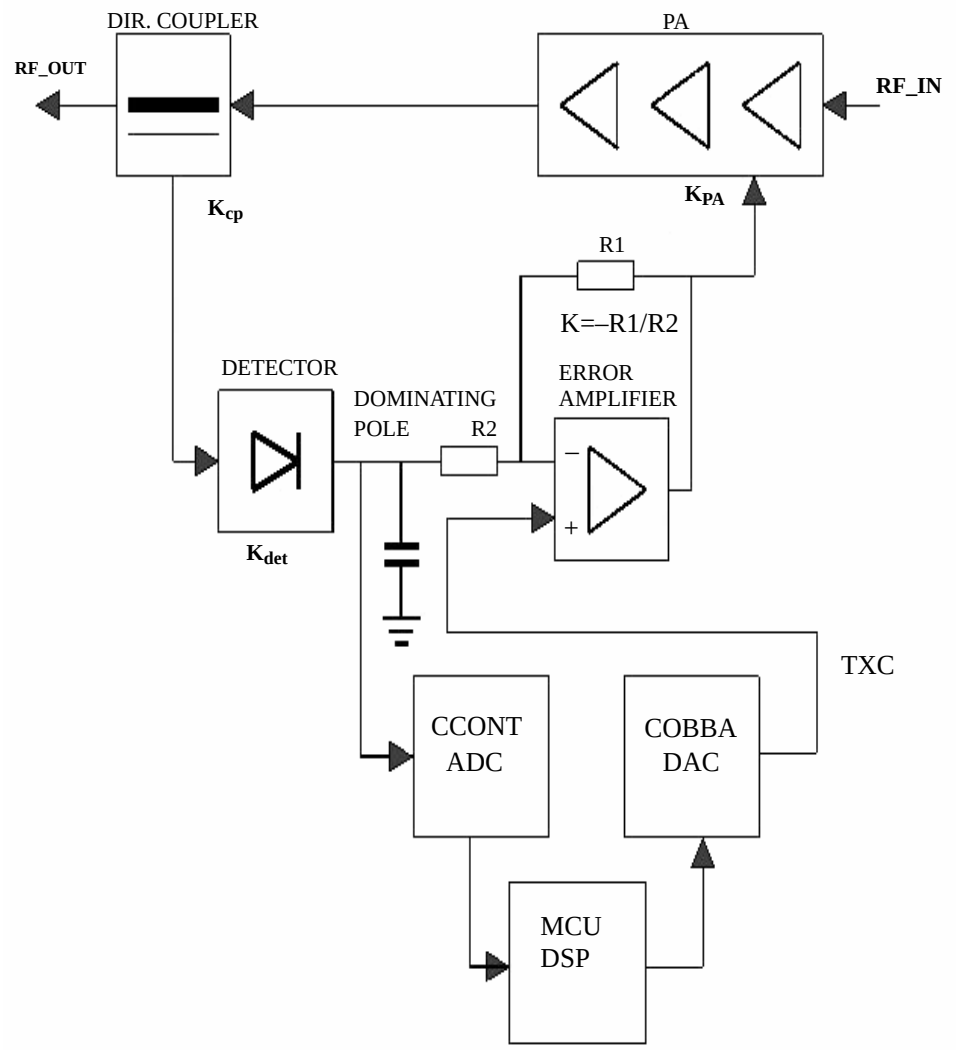


Figure 18: Power Control Loop

Frequency Synthesizers

A 13 MHz VCTCXO module is used as a stable reference for both the RF and BB circuitry. Temperature variations in the VCTCXO module are controlled by an AFC voltage, which is generated by a 11 bit D/A converter in COBBA_GJ. The output of the VCTCXO module feeds both the UHF PLL and the VHF PLL (both of which are located in SUMMA) and the BB circuitry for A/D conversion. The BB uses this information for frequency compensation algorithms.

The UHF synthesizers contains a 64/65 dual modulus prescaler, a ”N” and ”A” divider, a reference divide, a phase detector, a charge pump, a (VCO), and a lowpass filter. The UHF and VHF PLL are controlled with three serial busses; a data bus (SDATA), a serial clock bus (SCLK) and a latch enable (SLE). The UHF LO signal is generated by the UHF VCO module which has a tunable frequency range from 1443 MHz to 1510 MHz for the GSM1900 engine. A sample of the LO signal is fed to the 64/65 prescaler. The signal is then fed to the programmable dividers (N and A) which are programmed via the serial bus. This output then becomes one of the inputs to the phase detector. The other input to the phase

detector is a multiple of the 13MHz VCTCXO (reference frequency is 200 kHz). Output of the phase detector is connected to the charge pump, which charges or discharges the integrator capacitor in the loop filter depending on the phase of the measured frequency compared to reference frequency. The loop filter attenuates the pulses and generates a DC voltage which controls the frequency of UHF VCO. This loop filter defines the step response of the PLL (settling time), affects the stability of the loop and is used for side-band rejection.

The VHF synthesizers contains a 16/17 dual modulus prescaler, a "N" and "A" divider, a reference divide, a phase detector, a charge pump, a discrete VCO, and a lowpass filter. The frequency of the VHF VCO is 800 MHz, which is frequency divided to 400 MHz and 100 MHz. Operation of the VHF PLL is similar to that of the UHF PLL. The VHF PLL using the 400 MHz signal as its input frequency. The reference frequency in the VHF synthe-sizer is 1 MHz.

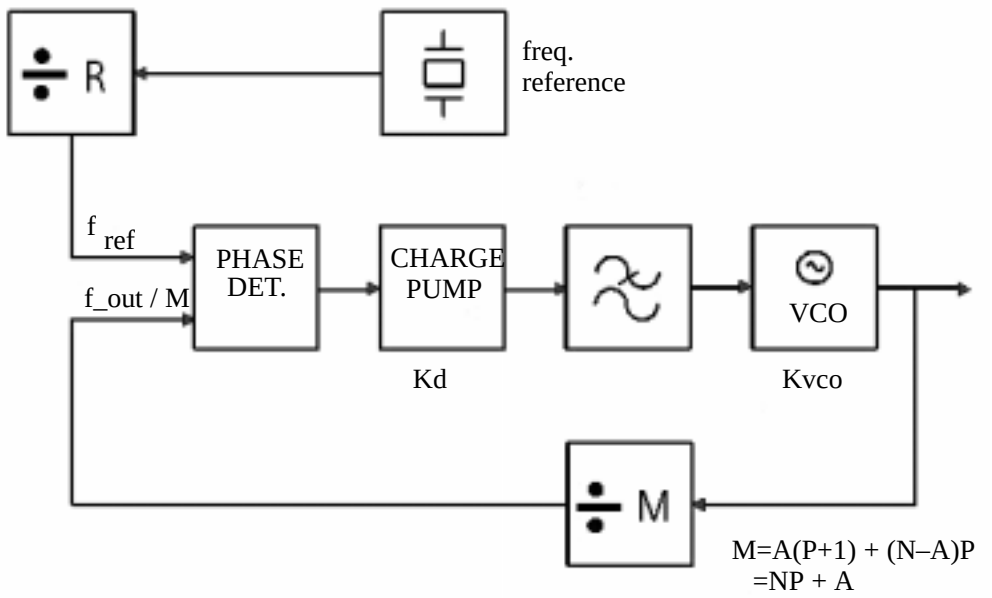


Figure 19: Phase Control Loop

AGC

The purpose of the AGC–amplifier is to maintain a constant output level from the receiver. To accomplish this, pre–monitoring is used. This premonitoring is done in three phases and this determines the settling times for the RX AGC. The receiver is switched on approximately 150 ms before the burst begins, DSP measures the receive signal level and adjusts the TXC–DAC (which controls Receive Controlled Gain Amplifier) or it switches on/off the LNA with the FRAC control line. The Receive Controlled Gain Amplifier has 57 dB of continuous gain control (40 dB to –17 dB) while the gain in the LNA is a digital step and is either 15 dB or –16 dB.

The requirement for receive signal level (RSSI) under static conditions is that the MS shall measure and report to the BS over the range –48 dBm to –110 dBm. For RF levels above –48 dBm, the MS must report to BS the same reading, so above this level the AGC is not required. Because of the RSSI requirements, the gain step in LNA is "ON" (FRAC = "0") for receive levels below –48 dBm. This leaves the AGC in SUMMA to adjust the gain

to desired value (50mVp–p). This is accomplished in DSP by measuring the receive IQ level after the selectivity filtering (IF–filters, SD–converter and FIR–filter in DSP). This results in an AGC dynamic range of 50 dB with the remaining 7 dB for gain variations in RX–chain (for calibration). For RF levels below –95 dBm, the output level of the receiver drops dB by dB with a level of 7.1 mVp–p @ –110 dBm for GSM1900.

This strategy is chosen because it is necessary to roll off the AGC in SUMMA early so that the signal is not saturated in selectivity tests but cannot roll off too early as this will sacrifice the signal to noise ratio, thus requiring a larger AGC dynamic range. The 50 mVpp target level is set, because the RX–DAC in COBBA_GJP will saturate at 1.4 Vpp. This results in over 28 dB of headroom which is required for the +/– 200 kHz faded adjacent channel (approximately 19 dB) and extra 9 dB for pre– monitoring.

AFC

The AFC is used to lock the MS clock to the frequency of the BS. AFC voltage is generated in COBBA_GJP with an 11 bit ADC. This voltage then controls the center frequency of the 13 MHz VCTCXO module.

Software Compensations

Power Levels (TXC) vs. Channel

Power levels are calibrated on one channel in production. Values for channels between these tuned channels are calculated using linear interpolation.

Modulator Output Level

For optimum linearity and efficiency, the output level of the modulator is adjusted in the production.

Power Levels vs temperature

In order to avoid the bias voltage variation of the detector diode ruining the accuracy of the power control loop, the bias voltage of the detector is measured when no RF power is transmitted. This voltage (DETLVL) is fed to the A/D converter in CCONT where DSP uses this value to correct the TXC voltage.

RSSI

Signal strength RSSI vs. input signal is calibrated in production, but RSSI vs. channel is compensated by software. If DETLVL (A/D) is used as a temperature sensor to correct for RX variations over temperature, the diode characteristics are 1.2mV/C.

TX power range

If COBBA_GJP does meet specifications, it will be necessary to divide the power levels into two ranges. One range will be between power level 0 to 10 (lets call this the HI range) with the other range between 11 and 15 (lets call this the LO range) . NOTE: at this time the exact range is unknown. One of MAD2_WD1 DSPGenOut pins will be used.

The TX power control range is divided into two regions for reasons of linearity in the

power sampling circuit and the ability of the software to reliably track multiple power levels during ramping. The two regions are from power level 15 through 7 and from 6 to 0. Provisions have been made in the service software to automatically track these break points in the calculation of the intermediate power levels.

RF Block Specifications

For further information on the different ASICs.
– CRFU_2a |5|
– SUMMA |6|
– COBBA_GJP |7|
– CCONT |3|
– MAD2_PR1 |8|
– CHAPS |9|

GSM1900 Duplex Filter

Table 18: Duplex filter

Parameter	Transmit section	Receive section	Unit
Passband	1850...1910	1930...1990	MHz
Maximum insertion loss in passband	2.0 (+25^{o} C) 2.2 (-30...+85^{o} C)	3.4 (+25^{o} C) 3.6 (-30...+85^{o} C)	dB
Maximum passband ripple	1.5	1.6	dB
Maximum VSWR	1.8	1.8	
Terminating impedance	50	50	ohms

Minimum attenuations	Freq. range	Att. (min)	Freq. range	Att. (min)	
	1930...1940	15	0...1100	50	MHz/dB
	1940...1990	17	1100...1700	35	MHz/dB
	3800...5730	32	1700...1830	30	MHz/dB
			1830...1910	20	MHz/dB
			2010...2070	10	MHz/dB
			2070...2700	25	MHz/dB
			2700...5000	20	MHz/dB
			5000...6000	15	MHz/dB

Parameter	Transmit section	Receive section	Unit
Average power	1		W
Weight	approximately 2		g
Package size (L x W x H)	10 x 17 x 4		mm

Receiver Blocks

LNA in CRFU_2a

Table 19: LNA requirements

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Frequency range	1930		1990	GHz
Gain	15.5	16.5	17.5	dB
NF		2.0		dB
HP3	-10	-8		dBm
1dB input compression point (AGC=H)	-18	-12		dBm
Absolute gain reduction @ 1900...2000MHz		34		dB
Relative step accuracy	-2		+2	dB/over temp. range
NF, when AGC-L			approxi-mately 1.8	dB
AGC settling time			1	us
Reverse isolation	18	21		dB

GSM1900 Receive Interstage Filter

Table 20: Electrical charactistics

Parameter	Min	Typ	Max	Unit/notes
Center frequency; **fo**	1960			MHz
Operating temperature range	-30...+85			deg. C
Passband	1930...1990			MHz
Terminating impedance	50			ohms
Insertion loss in passband		2.5	3.0	dB
Amplitude ripple in passband			1.0	dB
Return loss in passband	10			dB
Attenuation relative to **fo DC...900MHz**	20			dB
Attenuation relative to **fo** 900...1100MHz	45			dB
Attenuation relative to **fo** 1100...1700MHz	20			dB

Table 20: Electrical charactistics

Parameter	Min	Typ	Max	Unit/notes
Attenuation relative to **fo** 1700...1830MHz	12			dB
Attenuation relative to **fo** 1830...1910MHz	10			dB
Attenuation relative to **fo** 2010...2070MHz	3			dB
Attenuation relative to **fo** 2070...2200MHz	15			dB
Attenuation relative to **fo** 2200...5000MHz	30			dB
Attenuation relative to **fo** 5000...6000MHz	15			dB
Maximum drive level			0	dBm
Package LxWxH	3.0x3.0x2.0			mm
Vibration	Total amplitude 1.52 mm, 10-55MHz, 2 hours in each of 3 mutually perpendicular directions			mm

First Mixer (UHF) in CRFU_2a

First mixer is a double balanced Gilbert cell with a common base input stage. This mixer is optimized for being driven single ended. The performance of the mixer depends highly on the application and the mixer is therefore simulated with the ”real” circuit around it. The spread on the external components is included.

Table 21: First mixer specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input RF frequency	1930-1990			MHz
Output IF frequency		487		MHz
Power gain (see Note 1)	6.0		8.0	dB/GSM LO=1443-1503MHz
NF, SSB			11	dB
IIP3	-2			dBm
Input compression (1dB)	-10			dBm
1/2 IF spurious			n/a	dBm
LO-power in RF-input			-25	dBm
RF-IF isolation	20			dB

First IF Filter

The first IF filter is a SAW filter to improve the blocking conditions caused by inband spurious signals which cause a noise rice effect in second mixer if looser filter is used.

Table 22: First IF filter specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Operating temperature range		-30 ... +85		deg. C
Center frequency, *fo*		487		MHz
Maximum Ins. loss at 1dB BW		3.0	4.5	dB
Group delay ripple at 1dB BW			1.0	us pp
Bandwidth relative to *fo* 1dB bandwidth 10 dB bandwidth 13dB bandwidth 20 dB bandwidth 25 dB bandwidth 30 dB bandwidth	+/-200		+/-600 +/-800 +/-1000 +/-1600 +/-3000	kHz kHz kHz kHz kHz kHz
Spurious rejection, fo +/->5MHz	35			dB
Terminating impedance (balanced) input output		240//-0.4 330//-0.2		ohms//pF ohms//pF
Package size length x width (max) height (max)		3.8 x 3.8 1.8		mm mm
Assembly		SMD Reflow		

Second Mixer (VHF) in CRFU_2a

Second mixer is double balanced common emitter Gilbert cell. The mixer is optimized for differential drive; however, it can also be used with single ended drive. The LO-port is AC coupled internally.

Table 23: Second mixer specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input frequency		487		MHz
Output IF frequency		87		MHz
Input LO frequency		400		MHz
Input LO level	200		600	mVpp
LO input resistance	200			ohms/at400MHz

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Power gain	7		9	dB
NF, SSB driven differential			12	dB
IIP3 single ended	+4			dBm
Input compression (IdB)	-5.5			dBm
Input impedance		200		ohms
1/2 IF spurious Pin =-26dBm		-95	-80	dBm / 1/2IF at 443.5MHz
LO power in RF-input			-25	dBm

Table 24: Simulated typical values at lower temperatures (Note 1)

	25^{o} C	-20^{o} C	-30^{o} C
Gain	8 dB	8 dB	8 dB
NF	8.6 dB	7 dB	7 dB
ICP	-3 dBm		-4 dBm
HP3	12 dBm	10.5 dBm	10.5 dBm

NOTE 1: Typical gain and NF have been simulated at -20 degrees and -30 degrees for the s888g1. The figures in the table are for information only.

Second IF Filter

Table 25: Second IF filter specification

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Center frequency		87		MHz
Maximum ins. loss at 1 dBBW		9.0	11	dB
Amplitude ripple at 1 dBBW		1.5	2.0	Vpp
Group delay ripple at 1 dBBW			1.0	us pp
Bandwidth relative to 87 MHz 1 dB bandwidth 3 dB bandwidth 5 dB bandwidth 22 dB bandwidth 30 dB bandwidth 40 dB bandwidth	 +/-90 +/-120		 +/-230 +/-350 +/-550 +/-700	kHz
Spurious rejection, fo +/-26 MHz	65			dB
Terminating resistance		Input: 1.7 Output .9		k ohms

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Terminating capacitance		Input: 8.7 Output: 14.7		pF
Package L x W x H				mm

AGC and Third Mixer in SUMMA

Table 26: AGC and third mixer specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input frequency		87		MHz
Output frequency		13		MHz
Total noise figure, SSB, max. gain			15	dB/source=470W
Total noise figure, SSB, min. gain			65	dB/source=470W
Max. voltage gain	40			dB
Min. voltage gain			-20	dB
Total receiver absolute gain change over temperature in a unit, from SUMMA input to IF output (13MHz) for gains between 40 to 15 dB	-2		+2	dB
Total receiver absolute gain change over temperature in a unit, from SUMMA input to IF output (13MHz) for gains between 15 to -20 dB	-4		+4	dB
Control voltage for min. gain		0.5		V
Control voltage for max. gain		1.4		V
Gain control slope		85		dB/V
Compression point (1 dB) maximum gain	800			mVpp
Compression point (1 dB) minimum gain	80			mVpp
IF input impedance (balanced)	2.4	3.8/2	5.6	kohms/pF
Mixer output impedance (single ended)			100	ohms
Gain step up/down settling time			10	usec
Power OFF time			10	usec
Power ON time			10	usec
Mixer out to in isolation	45			dB

Third IF Filter

Table 27: Third IF filter specification

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Center frequency, fo		13		MHz
1 dB bandwidth; 1 dBBW	+/-90			kHz
Insertion loss			6.0	dB
Amplitude ripple at 1 dBBW			1.0	dB
Group delay ripple at 1 dBBW			1.5	µs p-p
Attentuations, relative to fo fo +/-400 kHz fo +/-600 kHz fo +/-800 KHz	 25 35 45			dB
Terminating impedance	313	330	347	ohms
Operating temperature range	-20		+75	C
Storage temperature range	-35		+85	C
Mechanical dimensions	L=7.3 W=3.3 H=1.8			mm

Third IF Buffer in SUMMA

Table 28: Third IF buffer specification

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Voltage gain (single ended input and balanced output)	34	36	38	dB
Maximum output level balanced (RL=10kW) (harmonics -20dBc)		1.4		Vpp
Input impedance		6//4		kohms//pF
Output impedance (single end)			300	ohms
Buffer out to IF in isolation	55			dB

Transmitter Block

IQ Modulator and TX AGC in SUMMA

Table 29: IQ modulator specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input frequency range	0		300	kHz

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input level (balanced)			1.2	Vpp
Input resistance (balanced)	200			kohms
Input capacitance (balanced)			4	pF
Input bias current (balanced)			100	nA
Input common mode voltage		0.8		V
IQ-input phase balance total, temperature included	-4		4	degrees
IQ-input phase balanced over temperature	-2		2	degrees
IQ-input gain balanced total, temperature included	-0.5		0.5	dB
IQ-input gain balance over temperature	-0.2		0.2	dB
Uncalibrated transmitter carrier suppression down to -40dBm wanted signal level		-20		dBc
Modulator Output	*Minimum*	*Typical/ Nominal*	*Maximum*	*Unit/Notes*
Output frequency		400		MHz
Max saturated output power into 100 ohm balanced load	-5	-3		dBm
Output power into 100 ohm balanced load used in HD955	-12	-10	-8	dBm
Absolute gain accuracy (process and temp variations)	-2		2	dB
Absolute gain change over temperature	-0.7		0.7	dB
Output noise level at max output power			-145	dBm/Hz
Output 3rd order intermod products when both wanted signals are at the level of -12dBm at the output			-35	dB
Power ON time			10	µsec
Power OFF time			10	µsec

Upconversion Mixer and Buffer in CRFU_2a

Table 30: Upconversion mixer and buffer specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input frequency		400		MHz
Output frequency range	1710		1910	MHz
Output level Pin=-15dBm”2dB	0	4	8	dBm
Relative gain variations over temp 25^{o}C /100^{o}C	-0.3		0	dB
Relative gain variations over temp 25^{o}C / -30^{o}C	0		+0.3	dB
Relative gain variations over Vdd 2.8V / 2.9V	-0.3		0	dB
Relative gain variations over Vdd 2.78V / 2.9V	0		-0.3	dB
Linear gain		20		dB
OIP3		15		dBm
NF SSB differentially		15	17	dB
LO rejection		-50	-15	dBc
2*LO rejection		-24	-20	dBc
3*LO rejection		-60	-35	dBc
4*LO rejection		-35	-30	dBc
IF rejection		-25	-22	dBc
2*IF rejection		-20	-16	dBc
3*IF rejection		-30	-25	dBc
4*IF rejection		-45	-35	dBc
2*IF rejection		-30	-25	dBc
Image rejection		-25	-15	dBc
2*Image rejection		-40	-32	dBc
2* LO - 3* IF		-45	-40	dBc
Input impedance		120-j170		ohms
Output VSWR to 50W			2	with external matching network

GSM1900 TX SAW Filter

Table 31: Electrical characteristics

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Passband	1850 - 1910			MHz
Terminating impedance	50			ohms
Insertion loss in passband			4.8	dB
Amplitude ripple in passband			2.8	dB
VSWR in passband			2.5	
Attenuation DC ... 1600 MHz	25	27		dB
Attenuation 1600 ... 1780 MHz	30	35		dB
Attenuation 1930 ... 1990 MHz	10	22		dB
Attenuation 2040 ... 2110 MHz	33	36		dB
Attenuation 2240 ... 2310 MHz	33	42		dB
Attenuation 2310 ... 5000 MHz	20	27		dB
Maximum drive level			+13	dBm

TX Buffer

Table 32: TX buffer specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Operating frequency range	1710		1910	
Gain	9	10	11	dB
NF			3	dB
Current consumption			20	mA
Output power (Z = 50W)		4	8	dBm
Input VSWR (Z = 50W)			2	
Output VSWR (Z = 50W)			2	

GSM1900 TX Ceramic Filter

Table 33: Electrical specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Center frequency; fo		1880		MHz
Operating temperature range	-30 ... +85			deg. C

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Passband	1850		1910	MHz
Terminating impedance		50		
Insertion loss in passband		3.0	4.0	dB
Amplitude ripple in passband		1.5	2.5	dB
Return loss in passband	8.0	10		dB
*Attenuation relative to fo DC ... 1600 MHz	30.0			dB
Attenuation relative to fo 1600 ... 1820 MHz	15			dB
Attenuation relative to fo 1930 ... 1990 MHz	5.0			dB
Attenation relative to fo 2100 ... 5000 MHz	20.0			dB
Drive level			10	dBm
Package L x W x H (max)		3.0 x 3.0 x 1.8		mm/SMD, reflow

Power Amplifier MMIC

Table 34: Power amplifier electrical specifications, 50 ohms

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Operating freq. range		GSM 1900 application circuit	1850		1910	MHz
Supply voltage	Vcc		3.0	3.5	5.0	V
Output power	Pout	Pin=0 dBm, Vcc=3.0V, Vpc=2.2V, Tamb=+25 deg. C	33			dBm
Gain control range (over-all dynamic range)		Vpc=0.5 ... 2.2V	45			dB
Gain control slope (sensi-tivity at the linear range)	8	Vpc1 @9V peak output volt Vpc2 @0.5V peak output volt S=(9-0.5)/(Vpc1-Vpc2)) V/V		60		V/V
Isolation		Vpc=0.2V, Pin=0 dbm			-40	dB
Carrier switching time	tr, tf	Pin=0 dBm Vpc is a pulse from 0.2 to 2.2V. Rise time up to -0.5 dB from the final power. Fall time vice versa.			1	us
Total efficiency: includes all supply currents	h	Pin=0 dBm, Pout=+33 dBm, Vcc=3.5, Tamb=+25 deg. C	45			%
Control current	Ipc				+/-3	mA

Parameter	Symbol	Test condition	Min	Typ	Max	Unit
Harmonics		Pin= +6 dBm Pout= +1.0 ... +33 dBm Vcc=3.5V			-35	dBc
Input VSWR Zin=50W	VSWRi1	Pin=0 ... +6 dBm Pout=+33.0 dBm			2:1	
	VSWRi2	Pin=0 ... +6 dBm Pout=+1.0 ... +33 dBm, Vpc adjusted for desired power levels			4:1	
Leakage current	Ileak	Vpc=0 V, with RF drive Pin=+6dBm,			10	uA
Output intermodulation attenuation: Ratio of the wanted power level to highest intermodulation power level	IMA out	Pint* = Poutwanted -44 dB Fint = Fwanted +/-800kHz IMA = Poutwanted - Poutin Poutwanted=+ ... +33dBm Vcc = 3.5V Tamb =+25C measurement BW = 300kHz	50			dB
Input intermodulation distortion	IMD in	Pinwanted =+6 dBm Finwanted = highest channel Pinint =-50 dBm Finint = Finwanted - 20 MHz Poutwanted = 33 dBm IMD = Poutint - Poutimd Vcc = 3.0V	2			dB
AM-PM conversion	Kp	Pin=-2.0 ... +6.0 dBm Pout= +1.0 ... +33 dBm Vpc adjusted for desired output power levels Vcc=3.0V			3	deg/ dB
Receive band noise power	Pn	Pintx = 0 dBm Pinrx =-174 dBm/Hz noise floor Pout=+1.0 ... +33.0 dBm, Vpc adjusted for desired output power levels Vcc=3.5V, Tamb=+25 deg.C RBW=100kHz, Freq. band: 1930 ... 1990 MHz			-80	dBm
Stability		Pin=-2,0 ... +6.0 dBm Vcc=3.0 ... 5.0V Vpc=0 ... 2.2V Load VSWR 10:1 in-band, all phases and 20:1 out-band, all phases	All spurious outputs more than 60dB below desired signal			
Load mismatch stress		Pin= 0 dBm, Vcc=5.0V, Pout=+33.0 dBm Load VSWR 20:1, all phases	No module damage			

** This unmodulated interfering CW signal is coupled to the output of the PA.*

Directional Coupler

Table 35: Directional coupler specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Frequency range	1850		1910	MHz
Impedance level of primary circuit		50		ohms
Impedance level of secondary circuit		200		ohms
VSWR on primary line			1.8	
Insertion loss			0.3	dB
Coupling	-15		-13	dB
Isolation	25			dB
Directivity		10		dB
Power capacity			2	W

Power Detector

Table 36: Power detector specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Frequency range	1850		1910	MHz
Error over temperature; includes coupler	-1		+1	%
Dynamic range	45			dB
Linear range (1)	35			dB
Bias current for detector diode		40		uA
Output voltage	0.1		2.2	V
Load resistance	10			kohms

Note 1: RF input voltage versus detected output voltage

Power Control Section in SUMMA, Closed Loop Characteristics

Table 37: Power control and closed loop specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Output voltage	0.5		2.2	V
Detector input voltage	0.1		2.2	V
TXC input voltage	0.1		2.2	V

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
TXP input voltage, LOW			0.5	V
TXP input voltage, HIGH	2.4			V
Opaout voltage if TXP=low & bit S18in control register is 0		0		V
opaout-output current driving capability	4			mA
OP1 output impedance		50		ohms
Offset of OP1 op.amp	-40		+40	mV
Temperature coefficient of the offset voltage		30		µV/C
TXC and TXP input resistance	18			kohms
TXC and TXP input capacitance		4		pF
Bandwidth	6			MHz
Open loop gain		20		dB
Closed loop gain		15		dB
Closed loop - 3 dB BW		70		kHz
Phase margin	45	60		degrees
Gain margin		30		dB

Synthesizer Blocks

VC(TC)XO, Reference Oscillator

Table 38: VC(TC)XO

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Center frequency		13		MHz
Operating temperature range	-20		+75	C
Storage temperature	-35		+85	C
Output voltage swing	800			mVpp
Load resistance		2		kohms
Load capacitance		10		pF
Frequency tolerance @ 25^{o} C	-1.0		+1.0	ppm
Frequency tolerance after reflow (@ 25^{o} C)	-2.0		+2.0	ppm

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Frequency stability over the temperature range (ref. @ 25^{o} C)	-5.0		+5.0	ppm
Frequency stability vs supply voltage (2.8_100mV)	-0.1		-0.1	ppm
Frequency stability vs load change (_10%)	-0.3		+0.3	ppm
Aging	-1.0		+1.0	ppm
Nominal voltage for center frequency		1.3		V
Control voltage range	0.3		2.3	V
Harmonics (with 2 kohm//10 pF)			-5	dBc
Control sensitivity	_14		_20	ppm/V
Startup time			1	msec
Phase noise			-130	dBc/Hz

VHF PLL in SUMMA

Table 39: VHF synthesizer specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Start up settling time			3.0	ms
Phase error			0.5	degrees/RMS
Sidebands +/- 1 MHz +/- 2 MHz +/- 3 MHz >+/- 3.0 MHz			 -70 -80 -80 -90	dBc

Table 40: VHF PLL specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input frequency range *	150		850	MHz
Input signal level	100			mVpp
Input resistance	No data available			kohms
Input capacitance		No data available		pF

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Phase comparison frequency			1	MHz
Charge pump output		0.5		mA
Sink to source current matching error of the charge pump			+/- 5	%
Charge pump current error			+/- 10	%
Charge pump min. output voltage		0.5		V
Charge pump max. output voltage		VCE-0.5		V
Charge pump leakage current			5	nA
Phase detector phase noise level			-163	dBc/Hz

* PLL is locked to 400MHz

VHF VCO and Lowpass Filter

Table 41: VHF VCO and lowpass filter specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Control voltage	0.5		4.0	V
Operation frequency		800		MHz
Output level	-7	-5	-3	dBm
Output impedance		50		ohms
Harmonics			-10	dBc
Phase noise, fo +/- 600 kHz fo +/- 1600 kHz fo +/- 3000 kHz			 -123 -133 -143	dBc
Control voltage sensitivity	8	9	10	MHz/V
Frequency Pulling Figures				
due to load variations			+/- 1	MHz
due to supply variations			+/- 1	MHz/V
due to temp variations			+/- 3	MHz, -20...+75

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Operating temperature	-10		75	C
Storage temperature	-40		85	C
Package	8.8 x 6.8 x 1.8 mm (max)			SMD reflow

UHF PLL

Table 42: UHF synthesizer specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Start up settling time			3.0	ms
Settling time +/- 83 MHz at operating frequency range		500	800	µs
Phase error			2	degrees/RMS
Sidebands +/- 200 kHz +/- 400 kHz +/- 600...+/-1400 kHz +/- 1.4...+/- 3.0 MHz >+/- 3.0 MHz			 -40 -60 -66 -76 -86	dBc

Table 43: UHF PLL in SUMMA specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input frequency range ADDBIAS off	650		1300	MHz
Input frequency range ADDBIAS on	650		1700	MHz
Input signal level (f<1300MHz)	200			mVpp
Input signal level (f>1300MHz) ADDBIAS must be on	300			mVpp
Reference input frequency		13		MHz
Reference input impedance		50		ohms
Phase comparison frequency		200		kHz
Charge pump output		0.3		mA

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Sink to source current matching error of the charge pump			+/- 5	%
Charge pump current error			+/- 10	%
Charge pump leakage current			5	nA
Phase detector phase noise level			-163	dBc/Hz

GSM1900 UHF VCO module

Table 44: UHF VCO specifications

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Control voltage (Vc)				V
Oscillation frequency	1443.2		1509.8	MHz
TX frequency range	1450.2		1509.8	MHz
RX frequency range	1443.2		1502.8	MHz
Tuning voltage at center frequency	2.0	2.25	2.5	V
Tuning voltage sensitivity	29	33	37	MHz/V
Output power level	-4.0			dBm
Output impedance		50		ohms
VSWR			2	
Phase noise, fo +/- 25 kHz fo +/- 600 kHz fo +/- 1600 kHz fo +/- 3000 kHz			 -100 -120 -130 -140	dBc/Hz
Pulling figure	-1		1	MHz
Pushing figure	-1		1	MHz
Frequency stability over temperature range	-3		3	MHz
Harmonics			-10	dBc
Spurious			-70	dBc
Input capacitance at Vc-pin			100	pF

Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Operating temperature	-10		75	C
Storage temperature	-40		85	C
Package	6.0 x 8.0 x 1.8 mm (max)			SMD reflow

UHF LO signal into CRFU_2a

Table 45: UHF LO buffer specifications

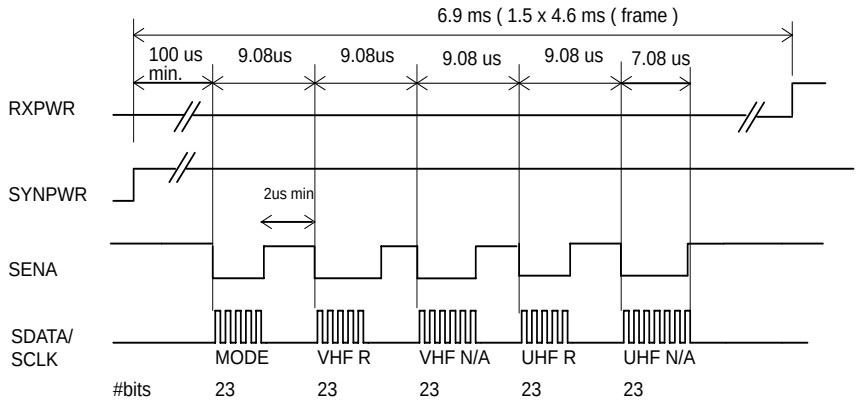
Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
Input frequency range GSM	1443		1510	MHz
Input level UHFLO_IN_P	-13 (140ohms)		-3 (261ohms)	dBm (measured input resistance)
Input level UHFLO_IN_M		N/A		This input is shorted to ground with a cap
Input impedance change between RX and TX mode			1	%
Start up time		10		usec
Input resistance		250		ohms
Input capacitance		No data available		pF
Phase noise, fo +/- 25 kHz fo +/- 600 kHz fo +/- 1600 kHz fo +/- 3000 kHz			 -100 -120 -130 -140	dBc/Hz
Pulling figure	-1		1	MHz
Pushing figure	-1		1	MHz
Frequency stability over temperature range	-3		3	MHz
Harmonics			-10	dBc
Spurious			-70	dBc
Input capacitance at Vc-pin			100	pF
Operating temperature	-10		75	C
Storage temperature	-40		85	C
Package	6.0 x 8.0 x 1.8 mm (max)			SMD reflow

Data Interface and Timing

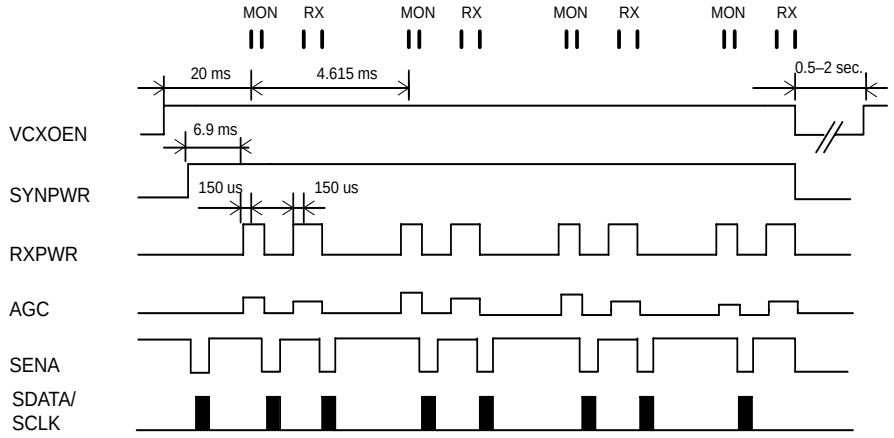
SUMMA is programmed via the serial bus SLE, SDAT, and SCLK. The data of SDAT is clocked by rising edge of SCLK. The data is fed MSB first and address bits before data bits. The data for the programmable dual modulus counter is fed first and the swallow counter last. SLE is kept low while clocking the data.

During programming, the charge pump attached to programmed divider is switched to high impedance state. Also, all counters connected to the PLL that is programmed are kept on reset while the SLE is low.

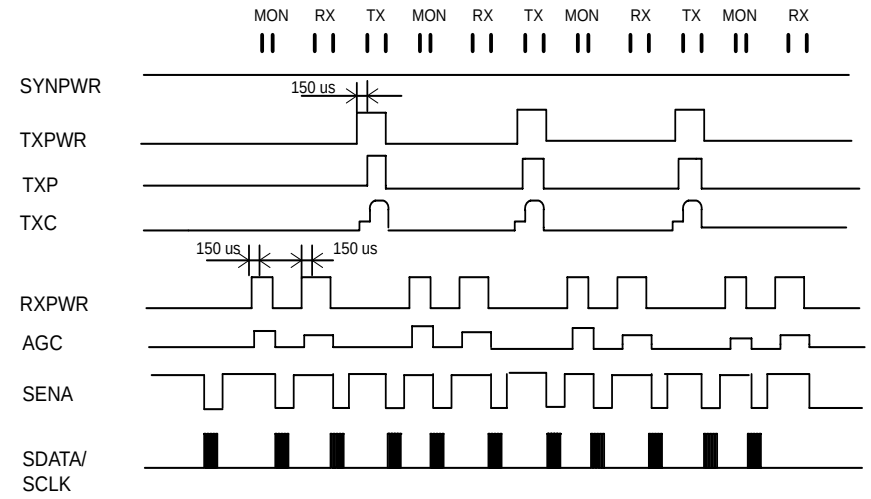
Synthesizer Timing Control



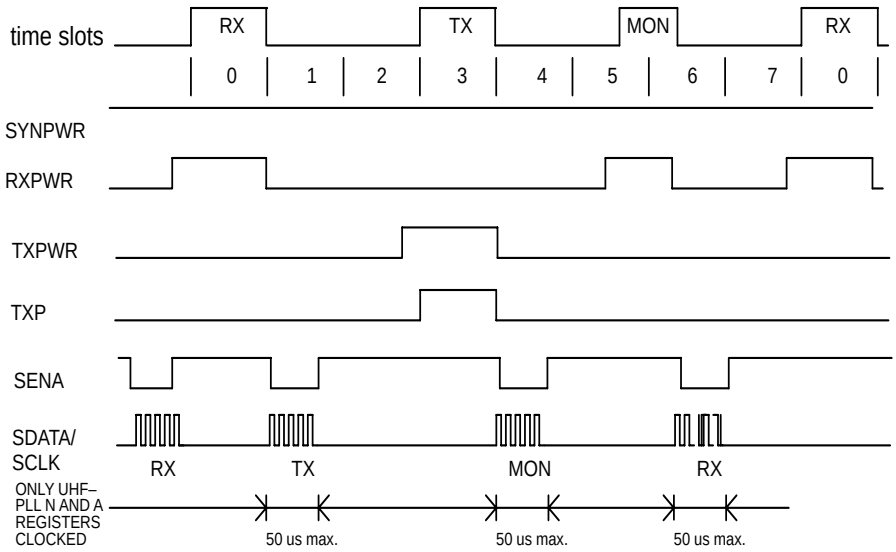
Synthesizer Start–up Timing / Clocking



Synthesizer Timing / IDLE one monitoring/frame,
frame can start from RX burst

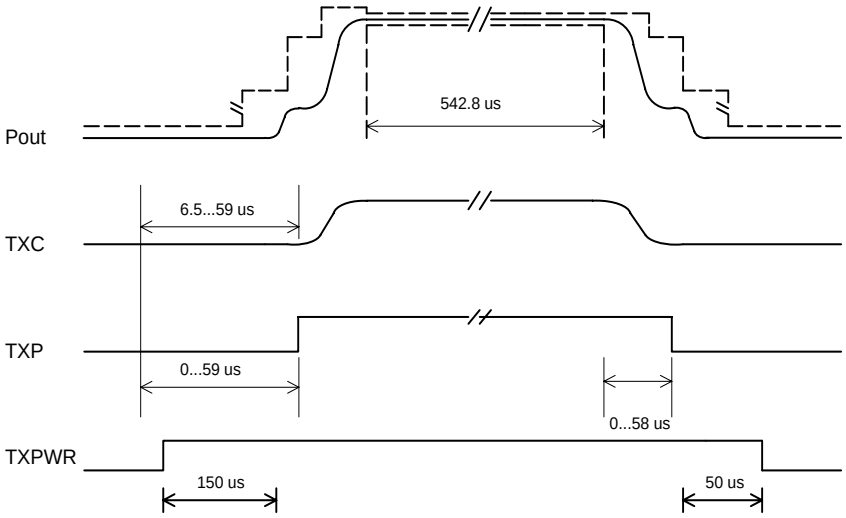


Synthesizer Timing / traffic channel



UHF–Synthesizer Timing / traffic channel

Transmit Power Timing



Transmitter Timing Diagram

Interfacing

The interfacing between RF and BB is comprised of the signals stated below:

SCLK	Clock for the PLL Serial Programming (3.25 MHz)
SDATA	Data for the PLL Serial Programming
SENA1	Latch Enable for the PLL Serial Programming
FRACTRL	Front-end Amplifier Control - Turns the gain in the LNA on and off
BAND_SEL	Band Selection - Selects between GSM 900 and GSM 1900 (i.e., it turns on the respective mixers and LNAs in the CRFU3
RXC	Receiver Gain Control - The control voltage for the AGC amplifier
AFC	Automatic Frequency Control Signal for the VCTCXO
RFC	A high stability clock signal for the logic circuits (13 MHz)
RXINN, RXINP	The differential RX signals to baseband
TXC	Transmitter power control signal, controls the shape of the burst
TXP	Transmitter power enable
TXIN, TXIP	Differential in-phase TX baseband signals for the RF modulator
TXQN, TXQP	Differential Quadrature-phase TX baseband signalsss for the RF modulator
VTX	Supply voltage for the TX chain, which also is used for control of the GSM 1900 TX/RX switch, together with BAND_SEL and VRX_1
VRX_1	Supply voltage for a part of the RX chain, which also is used for control of the GSM 1900 TX/RX switch

User Interface

The UI module includes the following:

- LEDs for backlight
- Plastic window
- Dust seal
- LCD adhesive
- Light guide
- Reflector
- Connector
- LCD cell (GD50) with display driver
- ON/OFF key
- Speaker connections.

The module is delivered as a single assembly (refer to *Disassembly* section).

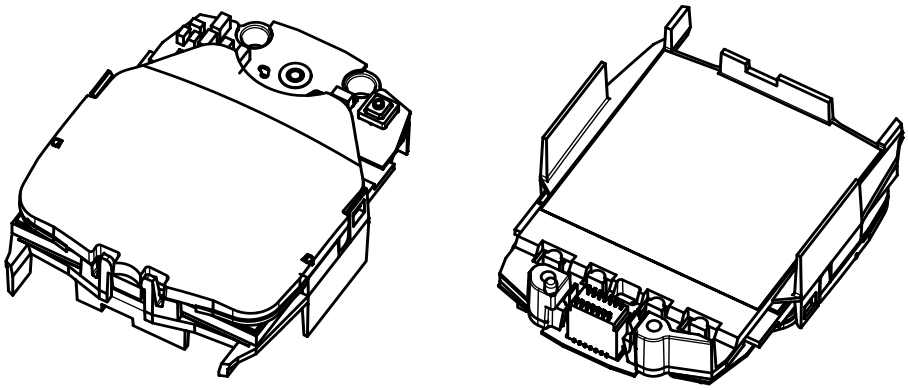


Figure 20: UI module assembled

LEDs

LEDs for the backlight of the LCD via the light guide are mounted on the back side of the module's FPC. There are four specially designed LEDs placed with a chip in the upper part of the LED.

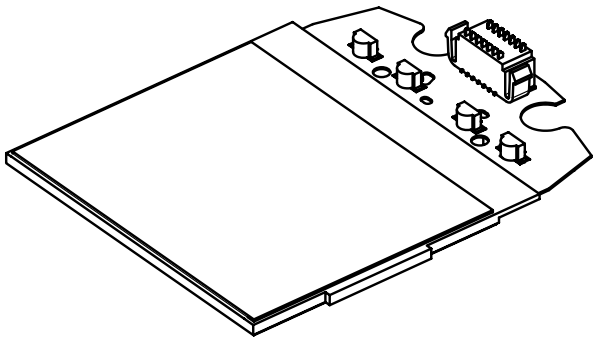


Figure 21: Mounting of LEDs for backlight (seen from underside)

Plastic Window

The window is mounted on top of the LCD module. It snaps into the light guide in three places. If a broken window needs to be replaced, it is replaced together with the dust seal.

Dust Seal

The dust seal is made of foam with adhesive backing on both sides. It keeps dust out of the LCD module and protects it from excessive pressure on the window, if pressed too hard. The dust seal is mounted inside the window and placed onto the LCD module. The window adhesive is high tack. The LCD adhesive is low tack to ease replacement of the window.

LCD Adhesive

This is a thin strip of foil with adhesive on both sides. It keeps the LCD module in place and protects it if the phone is dropped.

Reflector

The reflector is adhered to the underside of the light guide to reflect the backlight up to the viewing area. A thin adhesive border holds it in place and also keeps out dust.

Connector

The connector makes a mechanical connection between light guide and LCD, so the LCD can be clicked onto the light guide. Also, it makes electrical connection between LCD cell and PCB. The connector is not attached to the PCB, but the 14-pin connector contains springs and makes the contact.

Light Guide

The light guide houses and connects the LCD module to the PCB and backlights the display. Several snap fits locate the window and a board-to-board connector.

Evenly distributed backlighting is controlled by a graduated etched pattern. The pattern becomes rougher the further it gets from the LEDs. This is on the underside, in the visual area. The rest of the light guide is polished to minimize light losses in the system.

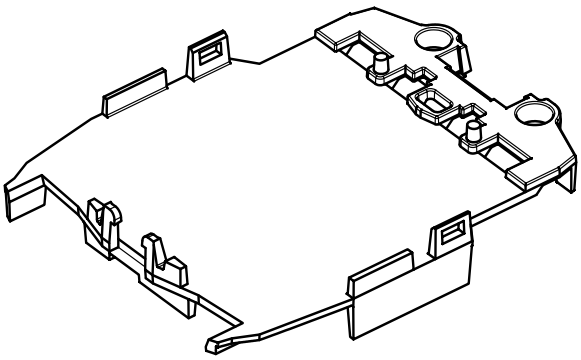


Figure 22: Light guide

The figure below shows the code marking for the light guide.

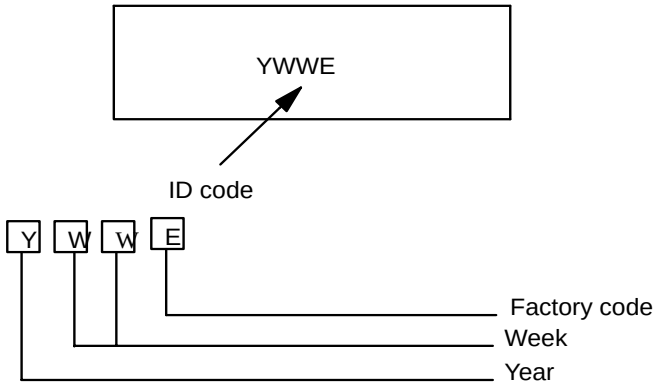


Figure 23: Marking specification for the light guide

UI Module Connection to Main PCB

Table 46: Module interface

Pin	Signal	Symbol	Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
1	Temp sensor		Temperature at LCD for compensation of contrast and brightness. Reference to GND.		47		kΩ NTC resistor @25^{0}C) Note: Not used in HD955
2	LDCDCX	tsas tsah	Control/display data flag input	150 150 low		 HIGH	ns/Setup time ns/Hold time Control data Display data
3	SPKR_p		Speaker connection	150			
4	LCDCSX	tcss tcsh	Chip select input, active low	 150 0.7xVDD		 0.2xVDD	ns ns V/HIGH V/LOW
5	SCL	 tscyc tshw tslw	Serial clock input	0 250 100 100		3.250	MHz/ VDD=2.7V ns ns ns
6	SPKR_n		Speaker connection				
7	ON/ OFF_key		ON/OFF key connection. Referenced to GND	0		VDD	V
8	LED-		LED negative connection		60		mA
9	LED+		LED positive connection		60		mA
10	ESD-GND	GND	GND		0		V
11	GND	GND	GND		0		V
12	VDD		Supply voltage	2.7 100	2.8	3.3 200	V uA/nominal supply volt., text on display @ 25^{0}C
13	SDA	tsds tsdh	Serial data input	 100			 ns

Table 46: Module interface

Pin	Signal	Symbol	Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
14	RES		Reset	1.0		0.2xVDD	V/LOW us/Reset

Signal	Symbol	Parameter	Minimum	Typical/ Nominal	Maximum	Unit/Notes
data signals	tr,tf				50	ns

Parts List

System Module (0201192)

(EDMS V8.7)

R100	1430788	Chip resistor	0w0622 k j	0402
R101	1825005	Chip varistor vwm14v vc30v		0805
R102	1419003	Chip resistor	0w5 0r22 j 200 ppm47 k j	1210
R103	1430796	Chip resistor	0w06 47 k j	0402
R104	1430770	Chip resistor	4.7 k	0402
R105	1430754	Chip resistor	0w06 1.0 k j	0402
R106	1419003	Chip resistor	0w06 47 k j	0402
R107	1430762	Chip resistor	0w06 2.2 k j	0402
R108	1430796	Chip resistor	0w06 47 k j	0402
R109	1430115	Chip resistor	0w06 2k2 f 200ppm	0402
R110	1430812	Chip resistor	0w06 220 k j	0402
R111	1430778	Chip resistor	0w06 10 k j	0402
R112	1430796	Chip resistor	0w06 47 k j	0402
R113	1430812	Chip resistor	0w06 220 k j	0402
R114	1430718	Chip resistor	0w06 47 r j	0402
R115	1620025	Resistor network	0w06 2x100 kj	0404
R116	1430754	Chip resistor	0w06 1.0 k	0402
R117	1430826	Chip resistor	0w06 680 k j	0402
R118	1430325	Chip resistor	0w06 2m2 j	0603
R119	1430754	Chip resistor	0w06 1.0 k	0402
R120	1620017	Resistor network	0w06 2x100 r j	0404
R121	1430726	Chip resistor	0w06 100 r j	0402
R123	1620019	Resistor network	0w06 2x10 k j	0404
R124	1430754	Chip resistor	0w06 1.0 k	0402
R125	1430778	Chip resistor	0w06 10 k j	0402
R126	1430796	Chip resistor	0w06 47 k j	0402
R128	1430762	Chip resistor	0w06 2.2 k j	
R129	1430754	Chip resistor	0w06 1.0 k	0402

R130	1430778	Chip resistor	0w06 10 k j	0402
R131	1825005	Chip varistor vwm14v vc30v		0805
R132	1430762	Chip resistor	0w06 2.2 k j	
R133	1825005	Chip varistor vwm14v vc30v		0805
R134	1430740	Chip resistor	0w06 330 r j	0402
R135	1430778	Chip resistor	0w06 10 k j	0402
R136	1825005	Chip varistor vwm14v vc30v		0805
R137	1430754	Chip resistor	0w06 1.0 k	0402
R138	1430135	Chip resistor	0w06 10 m j	0603
R200	1430804	Chip resistor	0w06 100 k j	0402
R201	1430804	Chip resistor	0w06 100 k j	0402
R202	1620103	Resistor network	0w06 2x22r j	0404
R300	1430804	Chip resistor	0w06 100 k j	0402
R301	1430700	Chip resistor	0w06 10 r j	0402
R302	1430762	Chip resistor	0w06 2.2 k j	
R303	1430762	Chip resistor	0w06 2.2 k j	
R306	1430812	Chip resistor	0w06 220 k j	0402
R307	1430796	Chip resistor	0w06 47 k j	0402
R308	1430796	Chip resistor	0w06 47 k j	0402
R309	1430804	Chip resistor	0w06 100 k j	0402
R350	1430762	Chip resistor	0w06 2.2 k j	
R351	1430804	Chip resistor	0w06 100 k j	0402
R352	1430778	Chip resistor	0w06 10 k j	0402
R353	1430754	Chip resistor	0w06 1.0 k	0402
R354	1620117	Resistor network	0w06 2x5r6 j	0404
R355	1620117	Resistor network	0w06 2x5r6 j	0404
R400	1430748	Chip resistor	0w06 470 r j	0402
R401	1430748	Chip resistor	0w06 470 r j	0402
R403	1430748	Chip resistor	0w06 470 r j	0402
R402	1430714	Chip resistor	0w06 33 r j	0402
R404	1430035	Chip resistor	0206 1k0 j	0603
R406	1430714	Chip resistor	0w06 33 r j	0402
R407	1430732	Chip resistor	0w06 180 r j	0402
R408	1430732	Chip resistor	0w06 180 r j	0402

R409	1430744	Chip resistor	0w06 470 r j	0402
R410	1430744	Chip resistor	0w06 470 r j	0402
R411	1430732	Chip resistor	0w06 180 r j	0402
R412	1430744	Chip resistor	0w06 470 r j	0402
R413	1430778	Chip resistor	0w06 10 k j	0402
R414	1430714	Chip resistor	0w06 33 r j	0402
R415	1430714	Chip resistor	0w06 33 r j	0402
R416	1430804	Chip resistor	0w06 100 k j	0402
R417	1825001	Chip varistor vwm 18v	vc40v	0603
R418	1825001	Chip varistor vwm 18v	vc40v	0603
R419	1430754	Chip resistor	0w06 1.0 k	0402
R420	1430754	Chip resistor	0w06 1.0 k	0402
R421	1430754	Chip resistor	0w06 1.0 k	0402
R422	1430754	Chip resistor	0w06 1.0 k	0402
R501	1430778	Chip resistor	0w06 10 k j	0402
R502	1430762	Chip resistor	0w06 2.2 k j	
R504	1430778	Chip resistor	0w06 10 k j	0402
R505	1430778	Chip resistor	0w06 10 k j	0402
R506	1430778	Chip resistor	0w06 10 k j	0402
R510	1430812	Chip resistor	0w06 220 k j	0402
R511	1430762	Chip resistor	0w06 2.2 k j	
R512	1430778	Chip resistor	0w06 10 k j	0402
R513	1430804	Chip resistor	0w06 100 k j	0402
R515	1430778	Chip resistor	0w06 10 k j	0402
R516	1430762	Chip resistor	0w06 2.2 k j	
R519	1430762	Chip resistor	0w06 2.2 k j	
R520	1430804	Chip resistor	0w06 100 k j	0402
R521	1430754	Chip resistor	0w06 1.0 k	0402
R523	1430762	Chip resistor	0w06 2.2 k j	
R524	1430762	Chip resistor	0w06 2.2 k j	
R525	1430726	Chip resistor	0w06 100 r j	0402
R528	1430762	Chip resistor	0w06 2.2 k j	
R531	1430762	Chip resistor	0w06 2.2 k j	
R532	1430754	Chip resistor	0w06 1.0 k	0402

R546	1430718	Chip resistor	0w06 47 r j	0402
R570	1419003	Chip resistor	0w06 47 k j	0402
R571	1430716	Chip resistor	0w06 39 r j	0402
R572	1430726	Chip resistor	0w06 100 r j	0402
R590	1430700	Chip resistor	0w06 10 r j	0402
R591	1430732	Chip resistor	0w06 180 r j	0402
R592	1430700	Chip resistor	0w06 10 r j	
R602	1419003	Chip resistor	0w06 47 k j	0402
R603	1419003	Chip resistor	0w06 47 k j	0402
R604	1430740	Chip resistor	0w06 330 r j	0402
R605	1430732	Chip resistor	0w06 180 r j	0402
R606	1430730	Chip resistor	0w06 150 r j	0402
R610	1430778	Chip resistor	0w06 10 k j	0402
R640	1430778	Chip resistor	0w06 10 k j	0402
R641	1430778	Chip resistor	0w06 10 k j	0402
R675	1430726	Chip resistor	0w06 100 r j	0402
R701	1430700	Chip resistor	0w06 10 r j	
R702	1430778	Chip resistor	0w06 10 k j	0402
R703	1419003	Chip resistor	0w06 47 k j	0402
R704	1430788	Chip resistor	0w0622 k j	0402
R705	1430762	Chip resistor	0w06 2.2 k j	
R706	1430762	Chip resistor	0w06 2.2 k j	
R707	1430812	Chip resistor	0w06 220 k j	0402
R708	1430700	Chip resistor	0w06 10 r j	
R711	1430732	Chip resistor	0w06 180 r j	0402
R712	1430778	Chip resistor	0w06 10 k j	0402
R714	1430754	Chip resistor	0w06 1.0 k	0402
R715	1430726	Chip resistor	0w06 100 r j	0402
R716	1430700	Chip resistor	0w06 10 r j	0402
R717	1430762	Chip resistor	0w06 2.2 k j	0402
R729	1419003	Chip resistor	0w06 47 k j	0402
R745	1430851	Chip resistor	0w06 15 k g 200ppm	0402
R755	1430716	Chip resistor	0w06 39 r j	0402

R756	1430706	Chip resistor	0w06 15 r j	0402
R757	1430716	Chip resistor	0w06 39 r j	0402
R758	1430778	Chip resistor	0w06 10 k j	0402
R759	1430700	Chip resistor	0w06 10 r j	0402
R760	1430740	Chip resistor	0w06 330 r j	0402
R834	1430710	Chip resistor	0w06 22 r j	0402
R835	1430744	Chip resistor	0w06 470 r j	0402
R836	1430693	Chip resistor	0w06 5r6 j	0402
R838	1430778	Chip resistor	0w06 10 k j	0402
R839	1430740	Chip resistor	0w06 330 r j	0402
R840	1430681	Chip resistor	0w06 4r3 j	0402
R842	1430726	Chip resistor	0w06 100 r j	0402
R846	1430730	Chip resistor	0w06 150 r j	0402
R847	1430700	Chip resistor	0w06 10 r j	0402
R848	1430700	Chip resistor	0w06 10 r j	0402
R849	1430718	Chip resistor	0w06 47 r j	0402
R850	1430706	Chip resistor	0w06 15 r j	0402
R851	1430706	Chip resistor	0w06 15 r j	0402
R852	1430706	Chip resistor	0w06 15 r j	0402
R853	1430690	Chip jumper	0r0	0402
R854	1430690	Chip jumper	0r0	0402
R855	1430690	Chip jumper	0r0	0402
R856	1430690	Chip jumper	0r0	0402
R857	1430690	Chip jumper	0r0	0402
C100	2320744	Chip cap x7r 1n0 k	50 v	0402
C101	2320536	Chip cap np0 10p j	50 v	0402
C103	2320546	Chip cap np0 27p j	50 v	0402
C104	2320540	Chip cap np0 15 p j	50 v	0402
C105	2320778	Chip cap x7r 10 n k	16 v	0402
C106	2320783	Chip cap x7r 33 n k	10 v	0402
C107	2320783	Chip cap x7r 33 n k	10 v	0402
C108	2320805	Chip cap x5r 100 n k	10 v	0402
C109	2320481	Chip cap x5r 1uk	6v3	0603
C110	2320805	Chip cap x5r 100 n k	10 v	0402

C111	2312411	Chip cap x5r 1u0 m	25 v	1206
C112	2320805	Chip cap x5r 100 n k	10 v	0402
C113	2320783	Chip cap x7r 33 n k	10 v	0402
C114	2320592	Chip cap x7r 2n2 j	50 v	0402
C115	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C116	2320805	Chip cap x5r 100 n k	10 v	0402
C117	2320783	Chip cap x7r 33 n k	10 v	0402
C118	2320783	Chip cap x7r 33 n k	10 v	0402
C119	2320778	Chip cap x7r 10 n k	16 v	0402
C120	2320778	Chip cap x7r 10 n k	16 v	0402
C121	2320783	Chip cap x7r 33 n k	10 v	0402
C122	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C123	2320131	Chip cap x7r 33n k	16 v	0603
C124	2320805	Chip cap x5r 100 n k	10 v	0402
C125	2320536	Chip cap np0 10p j	50 v	0402
C126	2320779	Chip cap x7r 100 n k	16 v	0603
C127	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C128	2310793	Chip cap x5r 2u2 k	10 v	0805
C129	2320536	Chip cap np0 10p j	50 v	0402
C130	2320560	Chip cap np0 100p j	50 v	0402
C131	2320560	Chip cap np0 100p j	50 v	0402
C133	2320536	Chip cap np0 10p j	50 v	0402
C134	2320481	Chip cap x5r 1uk	6v3	0603
C135	2320481	Chip cap x5r 1uk	6v3	0603
C136	2320805	Chip cap x5r 100 n k	10 v	0402
C137	2320481	Chip cap x5r 1uk	6v3	0603
C138	2320592	Chip cap x7r 2n2 j	50 v	0402
C139	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C140	2320805	Chip cap x5r 100 n k	10 v	0402
C141	2320481	Chip cap x5r 1uk	6v3	0603
C142	2320805	Chip cap x5r 100 n k	10 v	0402
C143	2312401	Chip cap x5r 1u0 k	10 v	0805
C144	2320536	Chip cap np0 10p j	50 v	0402
C145	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	

C146	2320778	Chip cap x7r 10 n k	16 v	0402
C147	2320546	Chip cap np0 27p j	50 v	0402
C148	2320783	Chip cap x7r 33 n k	10 v	0402
C149	2320744	Chip cap x7r 1n0 k	50 v	0402
C150	2320508	Chip cap np0 1p0 c	50 v	0402
C151	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C152	2320744	Chip cap x7r 1n0 k	50 v	0402
C153	2320137	Chip cap x5r 470n k	10 v	0603
C154	2320546	Chip cap np0 27p j	50 v	0402
C155	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C156	2320536	Chip cap np0 10p j	50 v	0402
C157	2320536	Chip cap np0 10p j	50 v	0402
C158	2320536	Chip cap np0 10p j	50 v	0402
C161	2320778	Chip cap x7r 10 n k	16 v	0402
C162	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C163	2320536	Chip cap np0 10p j	50 v	0402
C164	2320536	Chip cap np0 10p j	50 v	0402
C165	2320536	Chip cap np0 10p j	50 v	0402
C166	2320744	Chip cap x7r 1n0 k	50 v	0402
C167	2320536	Chip cap np0 10p j	50 v	0402
C168	2320536	Chip cap np0 10p j	50 v	0402
C169	2320536	Chip cap np0 10p j	50 v	0402
C170	2320536	Chip cap np0 10p j	50 v	0402
C171	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C172	2320536	Chip cap np0 10p j	50 v	0402
C173	2320778	Chip cap x7r 10 n k	16 v	0402
C174	2320536	Chip cap np0 10p j	50 v	0402
C175	2320536	Chip cap np0 10p j	50 v	0402
C176	2610003	Chiptcap 10u m10 v	3.2x1.6x1.6	
C200	2320783	Chip cap x7r 33 n k	10 v	0402
C201	2320620	Chip cap x7r 10 n j	16 v	0402
C202	2320620	Chip cap x7r 10 n j	16 v	0402
C203	2320536	Chip cap np0 10p j	50 v	0402
C204	2320536	Chip cap np0 10p j	50 v	0402

C300	2320744	Chip cap x7r 1n0 k	50 v	0402
C302	2320778	Chip cap x7r 10 n k	16 v	0402
C303	2320805	Chip cap x5r 100 n k	10 v	0402
C304	2320778	Chip cap x7r 10 n k	16 v	0402
C306	2320778	Chip cap x7r 10 n k	16 v	0402
C307	2320778	Chip cap x7r 10 n k	16 v	0402
C308	2320481	Chip cap x5r 1uk	6v3	0603
C309	2320481	Chip cap x5r 1uk	6v3	0603
C310	2320481	Chip cap x5r 1uk	6v3	0603
C311	2320481	Chip cap x5r 1uk	6v3	0603
C312	2320805	Chip cap x5r 100 n k	10 v	0402
C350	2320536	Chip cap np0 10p j	50 v	0402
C351	2320481	Chip cap x5r 1uk	6v3	0603
C352	2320536	Chip cap np0 10p j	50 v	0402
C353	2320805	Chip cap x5r 100 n k	10 v	0402
C354	2320546	Chip cap np0 27p j	50 v	0402
C356	2320805	Chip cap x5r 100 n k	10 v	0402
C400	2320620	Chip cap x7r 10 n j	16 v	0402
C401	2320620	Chip cap x7r 10 n j	16 v	0402
C402	2320620	Chip cap x7r 10 n j	16 v	0402
C404	2320536	Chip cap np0 10p j	50 v	0402
C405	2320536	Chip cap np0 10p j	50 v	0402
C500	2320536	Chip cap np0 10p j	50 v	0402
C501	2320546	Chip cap np0 27p j	50 v	0402
C502	2320546	Chip cap np0 27p j	50 v	0402
C511	2320744	Chip cap x7r 1n0 k	50 v	0402
C514	2320536	Chip cap np0 10p j	50 v	0402
C516	2320536	Chip cap np0 10p j	50 v	0402
C517	2320560	Chip cap np0 100p j	50 v	0402
C518	2320536	Chip cap np0 10p j	50 v	0402
C519	2320536	Chip cap np0 10p j	50 v	0402
C520	2611668	Chiptcap 4u7 m 10 v	3.2x1.6x1.6	
C521	2320778	Chip cap x7r 10 n k	16 v	0402
C522	2320560	Chip cap np0 100p j	50 v	0402

C524	2320584	Chip cap x7r 1n0 j	50 v	0402
C525	2320548	Chip cap np0 33 p j	50 v	0402
C526	2320548	Chip cap np0 33 p j	50 v	0402
C527	2320584	Chip cap x7r 1n0 j	50 v	0402
C531	2320576	Chip cap x7r 470p j	50 v	0402
C535	2320546	Chip cap np0 27p j	50 v	0402
C536	2320546	Chip cap np0 27p j	50 v	0402
C539	2320546	Chip cap np0 27p j	50 v	0402
C540	2320546	Chip cap np0 27p j	50 v	0402
C541	2320560	Chip cap np0 100p j	50 v	0402
C545	2320584	Chip cap x7r 1n0 j	50 v	0402
C561	2320516	Chip cap np0 1p5 c	50 v	0402
C562	2320564	Chip cap np0 150 p j	50 V	0402
C563	2320520	Chip cap np0 2p2 c	50 v	0402
C572	2320518	Chip cap np0 1p8 c	50 v	0402
C574	2320518	Chip cap np0 1p8 c	50 v	0402
C575	2320520	Chip cap np0 2p2 c	50 v	0402
C577	2320520	Chip cap np0 2p2 c	50 v	0402
C579	2320540	Chip cap np0 15 p j	50 v	0402
C581	2320744	Chip cap x7r 1n0 k	50 v	0402
C583	2320744	Chip cap x7r 1n0 k	50 v	0402
C584	2320540	Chip cap np0 15 p j	50 v	0402
C585	2320744	Chip cap x7r 1n0 k	50 v	0402
C587	2320540	Chip cap np0 15 p j	50 v	0402
C588	2320540	Chip cap np0 15 p j	50 v	0402
C601	2320911	Chip cap np0 hq 1p5 b	25 v	0402
C602	2320744	Chip cap x7r 1n0 k	50 v	0402
C603	2320524	Chip cap np0 3p3 c	50 v	0402
C605	2320516	Chip cap np0 1p5 c	50 v	0402
C606	2320516	Chip cap np0 1p5 c	50 v	0402
C609	2320536	Chip cap np0 10p j	50 v	0402
C611	2320744	Chip cap x7r 1n0 k	50 v	0402
C612	2320556	Chip cap np0 68 p j	50 v	0402
C613	2320556	Chip cap np0 68 p j	50 v	0402

C614	2320752	Chip cap x7r 2n2 k	50 v	0402
C616	2320584	Chip cap x7r 1n0 j	50 v	0402
C617	2320584	Chip cap x7r 1n0 j	50 v	0402
C618	2320778	Chip cap x7r 10 n k	16 v	0402
C619	2320752	Chip cap x7r 2n2 k	50 v	0402
C620	2320560	Chip cap np0 100p j	50 v	0402
C621	2320532	Chip cap np0 6p8 c	50 v	0402
C622	2320532	Chip cap np0 6p8 c	50 v	0402
C623	2320939	Chip cap np0 hq 10 p f	16 v	0402
C624	2320564	Chip cap np0 150 p j	50 V	0402
C640	2320099	Chip cap x7r 4n7 j	50 v	0603
C641	2320099	Chip cap x7r 4n7 j	50 v	0603
C671	2320546	Chip cap np0 27p j	50 v	0402
C700	2320546	Chip cap np0 27p j	50 v	0402
C702	2320560	Chip cap np0 100p j	50 v	0402
C703	2310223	Chip cap np0 3n3 j	50 v	1206
C704	2320778	Chip cap x7r 10 n k	16 v	0402
C705	2320560	Chip cap np0 100p j	50 v	0402
C706	2320481	Chip cap x5r 1uk	6v3	0603
C707	2320738	Chip cap x7r 470p k	50 v	0402
C708	2310248	Chip cap np0 4n7 j	50 v	1206
C709	2320544	Chip cap np0 22 p j	50 v	0402
C711	2320939	Chip cap np0 hq 10 p f	16 v	0402
C714	2611749	Chiptcap 6u8 m 10 v	2.0x1.35x1.35	
C715	2320548	Chip cap np0 33 p j	50 v	0402
C716	2320560	Chip cap np0 100p j	50 v	0402
C718	2320536	Chip cap np0 10p j	50 v	0402
C719	2320536	Chip cap np0 10p j	50 v	0402
C720	2320778	Chip cap x7r 10 n k	16 v	0402
C721	2611749	Chiptcap 6u8 m 10 v	2.0x1.35x1.35	
C722	2320744	Chip cap x7r 1n0 k	50 v	0402
C724	2610027	Chiptcap 3u3 k 16 v	3.2x1.6x1.6	
C728	2312401	Chip cap x5r 1u0 k	10 v	0805
C730	2320744	Chip cap x7r 1n0 k	50 v	0402

C731	2320524	Chip cap np0 3p3 c	50 v	0402
C732	2320540	Chip cap np0 15 p j	50 v	0402
C734	2312401	Chip cap x5r 1u0 k	10 v	0805
C735	2611749	Chiptcap 6u8 m 10 v	2.0x1.35x1.35	
C759	2320560	Chip cap np0 100p j	50 v	0402
C760	2320744	Chip cap x7r 1n0 k	50 v	0402
C761	2320546	Chip cap np0 27p j	50 v	0402
C762	2611749	Chiptcap 6u8 m 10 v	2.0x1.35x1.35	
C771	2320546	Chip cap np0 27p j	50 v	0402
C772	2320911	Chip cap np0 hq 1p5 b	25 v	0402
C773	2320546	Chip cap np0 27p j	50 v	0402
C774	2320913	Chip cap tf np0 hq 1p8 b 25v		0402
C775	2320530	Chip cap np0 5p6 c	50 v	0402
C776	2320540	Chip cap np0 15 p j	50 v	0402
C787	2320805	Chip cap x5r 100 n k	10 v	0402
C788	2320901	Chip cap tf np0 hq 1p0 b 25 v		0402
C817	2320939	Chip cap np0 hq 10 p f 16 v		0402
C820	2320522	Chip cap np0 2p7 c	50 v	0402
C826	2320744	Chip cap x7r 1n0 k	50 v	0402
C828	2320915	Chip cap tf np0 hq 2p2 b 25 v		0402
C834	2611689	Chiptcap 470u m 10 v l 7.3x4.3x4.1		
C836	2320568	Chip cap x7r 220 p j	50 v	0402
C837	2320560	Chip cap np0 100p j	50 v	0402
C840	2320540	Chip cap np0 15 p j	50 v	0402
C841	2320536	Chip cap np0 10p j	50 v	0402
C842	2320907	Chip cap np0 hq 0p7 b	16 v	0402
C843	2320907	Chip cap np0 hq 0p7 b	16 v	0402
C845	2320524	Chip cap np0 3p3 c	50 v	0402
C851	2320939	Chip cap np0 hq 10 p f 16 v		0402
C852	2320901	Chip cap tf np0 hq 1p0 b 25 v		0402
L100	3203701	Ferrite bead 33r/100mhz		0805
L102	3203701	Ferrite bead 33r/100mhz		0805
L500	4551017	Dir.coupler 1890 +/-20mhz/15bd		2x1.4
L503	3645105	Chip coil 27nh j q12/100mhz		0603

L560	3645071	Chip inductor-0805hq	series HD955	
L601	3646007	Chip coil 27n j q27/800mhz		0402
L602	3646007	Chip coil 27n j q27/800mhz		0402
L603	3645183	Chip coil 56n j q12/100mhz		0603
L607	3645037	Chip coil 150nh k q15/25mhz		0603
L608	3645037	Chip coil 150nh k q15/25mhz		0603
L609	3645037	Chip coil 150nh k q15/25mhz		0603
L655	3203709	Ferrite bead 0.5r 120r/100m		0402
L700	3645105	Chip coil 27nh j q12/100mhz		0603
L701	3641206	Chip coil 3u3h k q25/7.96mhz		1008
L703	3645193	Chip coil 18n j q12/100mhz		0603
L710	3203701	Ferrite bead 33r/100mhz		0805
L711	3203709	Ferrite bead 0.5r 120r/100m		0402
L716	3203709	Ferrite bead 0.5r 120r/100m		0402
L718	3203709	Ferrite bead 0.5r 120r/100m		0402
L719	3203709	Ferrite bead 0.5r 120r/100m		0402
L720	3203709	Ferrite bead 0.5r 120r/100m		0402
L721	3646055	Chip coil 8n2 j q28/800mhz		0402
L722	3646055	Chip coil 8n2 j q28/800mhz		0402
L723	3646059	Chip coil 5n6 +/-0n3	q28/800m	0402
L725	3646005	Chip coil 2n7 +/-0n3	q29/800m	0402
B100	4510243	Crystal 32.768khz +/-20ppm 12.5 pf		
G700	4350227	Vco 1443-1510mhz	12ma	dcs
G701	4510217	VCTCXO 13.000mhz +/-5ppm 2.8v		
G702	4350229	Vco 800mhz 2.7v	7ma dcs	8.8x6.8
Z101	3640035	Filt z>450r/100m	0r7max 0.2a	0603
Z102	3640035	Filt z>450r/100m	0r7max 0.2a	0603
Z103	3640035	Filt z>450r/100m	0r7max 0.2a	0603
Z104	3640035	Filt z>450r/100m	0r7max 0.2a	0603
Z105	3640035	Filt z>450r/100m	0r7max 0.2a	0603
Z502	4512123	Dupl 1850-1910/1930-1990mhz		17x11
Z503	4511023	Saw filt 1880 +/-30mhz/4.2db		3x3
Z602	4550113	Cer.filt 1960 +/-30mhz/3.7db		5.9x4.4
Z603	4550111	Cer.filt 1880 +/-30mhz/3.7db		5.9x4.6

Z621	4511033	Saw filt 487 +/-0.2mhz/4.5db		4x4
Z700	4511001	Saw filt 87 +/-0.12mhz/10db		14.2x8.4
Z701	4510009	Cer.filt 13+/-0.09mhz	7.2x3.2	
V100	4113611	Emi filt/tvs emif01-10005w5		sot353
V101	4113611	Emi filt/tvs emif01-10005w5		sot353
V102	4113611	Emi filt/tvs emif01-10005w5		sot353
V103	4210215	Tr mmbt589 p 30v 1a	0.3w 80	sot23
V104	4110067	Sch di mbr0520l	20v 0.5a	sod123
V105	4110601	Di fast 1ss355 80V0.1a<4ns		sod323
V106	4113611	Emi filt/tvs emif01-10005w5		sot353
V107	4110601	Di fast 1ss355 80V0.1a<4ns		sod323
V108	4210100	Tr bc848w n 30v 0.1a	100mhz	sot323
V109	4211621	Mfetx2 fdg6322c	bip.replac	sot363
V110	4210100	Tr bc848w n 30v 0.1a	100mhz	sot323
V111	4113671	Tvs esda6v1w5	**no new design **	
V350	4210052	Tr dtc114ee n rb=rbe=10k		em3
V351	4210102	Tr bc858w p 30v 100ma 200mw		sot323
V400	4860005	LED cl270yg yelgrn>5mcd20ma		0603
V401	4860005	LED cl270yg yelgrn>5mcd20ma		0603
V402	4860005	LED cl270yg yelgrn>5mcd20ma		0603
V403	4860005	LED cl270yg yelgrn>5mcd20ma		0603
V404	4860005	LED cl270yg yelgrn>5mcd20ma		0603
V405	4860005	LED cl270yg yelgrn>5mcd20ma		0603
V406	4200836	Tr bcx19 n 50v 0.5a 200mhz		sot23
V407	4100278	Dix2 bav70 70v 200ma com-cat.sot23		
V408	4200836	Tr bcx19 n 50v 0.5a 200mhz		sot23
V409	4200836	Tr bcx19 n 50v 0.5a 200mhz		sot23
V410	4110601	Di fast 1ss355 80V0.1a<4ns		sod323
V411	4113671	Tvs esda6v1w5	**no new design **	
V501	4110079	Schdix2 hsms282c	15v <1pf	sot323
V506	4208607	Fet bss138 n 50 v 0.2a		sot23
V507	4210052	Tr dtc114ee n rb=rbe=10k		em3
V508	4112451	Pindi bar63-03w 50v 0.1a		sod323
V509	4210052	Tr dtc114ee n rb=rbe=10k		em3

V510	4210074	Tr bfp420 n 4.5v35ma	20ghz	sot343
V511	4210052	Tr dtc114ee n rb=rbe=10k		em3
V702	4210100	Tr bc848w n 30v 0.1a	100mhz	sot323
V720	4210074	Tr bfp420 n 4.5v35ma	20ghz	sot343
V808	4210015	Tr bfp405 n 4.5v12ma 20ghz		sot343
D100	4340387	Tc7w66fu 2xbilateral switch		ssop8
D300	4370593	Mad2wd1 v9/11 f731635a/b		ubga144
D301	4340597	Flash 2mx16 115ns 2.7v b3		ubga48
D302	4340681	Sram 512kx8 100ns	3.3v	stsop32
D303	4340585	Flash 1mx16 110ns 2.7v b3a		ubga48
D304	4340761	Mc33464n mcu reset 3.0v		sot23-5
D350	4340369	Tc7w126fu dual bus buffer		ssop8
N100	4370719	Ccont 2m wfd163	mg64t/8	lfbga8x8
N101	4370697	Uba2006t chaps charge control		so16
N200	4370643	Cobba_gjp v4.1 v257	bg64t/8	bga64
N350	4860031	tfdu4100 irda tx/rx>2.7v 115 kbits		
N500	4370649	Rf9126 pw amp	dcs1900	pssop-16
N600	4370245	Crfu2a_v3 comrfunit>2.7v		tssop28
N700	4370351	Summa v2 wfd167ct48t		tqfp48
F100	5119019	Sm fuse f 1.5a 32v		0603
S416	5409077	Sm push button sw spst 15v 20ma		
X100	5409065	Sm sim card conn	2x3pol	p2.54
X101	5496069	Sm batt conn 2pol spr p3.5 100v2a		
X102	5496069	Sm batt conn 2pol spr p3.5 100v2a		
X200	5469061	Sm system conn 6af+3dc+mic+jack		
X501	5429007	Sm coax conn m sw 50r 0.4-2ghz		
A001	9517067	Tx-Rx shield assy	dmc01679	HD955
A002	9517066	Oscil.shield assy	dmc01681	HD955
A003	9517067	Tx-Rx shield assy	dmc01679	HD955
	9380753	Bar code label	dmd03311	27x6.5
	9510602	Lna shield assy	dmc02393	HD955
	9854281	Pcb ur5 40.5x118.7x1.0 m8 4/pa		